ADVANTEST®

ADVANTEST CORPORATION

T5592

MEMORY TEST SYSTEM

PRODUCT DESCRIPTION

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Applicable System
T5592

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PREFACE

This manual provides general technical information on the Advantest Corporation T5592 memory test system. It covers the specifications of each memory test system.

For details on system performance and configuration, refer to the relevant manuals.

When there is a difference between this manual and the individual specification, the individual specifications take precedence.

RECORD OF REVISIONS

Manual Rev	Date	Remarks
01	Mar 31/00	
02	Apr 28/00	
03	Sep 12/00	
04	Feb 9/01	

Manual Rev	Date	Remarks

1. INTRODUCTION

1.1 General Description

The ADVANTEST T5592 is a general-purpose, high-performance and high-speed memory test system. This system has been designed to meet various requirements for the design of new generation VLSI memories and evaluation of their characteristics, and for the production of high-speed memories.

This system can be used to test and characterize ASMs (Application Specific Memories) --- such as multi-port memories, field memories, line memories, or other memories with specific applications --- and memory modules, as well as RDRAMs, SDRAMs, DRAMs, SRAMs, and other general-purpose memories.

During functional tests at a maximum test rate of 1.066 GHz in T5592, the system ensures high timing accuracy, high repeatability, and high fault detectability.

In order to meet the needs of increasing test time resulting from the growing memory capacity, this system allows up to 64 at two stations, and ensures high productivity. In addition to the capabilities for various types of functional tests, highly accurate timing and reference levels are provided, which allows testing of CMOS, TTL and other devices at a newly developed BiCMOS station. The high-speed and high-performance driver of the BiCMOS station permits testing of RSL, SSTL, GTL, ECL, and other small amplitude interfaces.

This system is shown in Figure 1-1.

Figure 1-1 T5592 Memory Test System

1.2 System Features

This system provides the highest test reliability, fault detection performance, and evaluation performance of the overall device characteristics through integration of various software packages that can operate on the general-purpose OS of single architecture provided by ADVANTEST.

Main features of the system are described below.

1.2.1 Flexible Algorithmic Pattern Generator (ALPG)

When testing VLSI memories with increased capacity, a more flexible, powerful algorithmic pattern generator is required for obtaining high fault detection capabilities while reducing the testing time.

In a functional test pattern, enhancement of fault detectability and reduction of testing time are in a mutually conflicting relationship. It is therefore important to reduce testing time without deteriorating the fault detectability, by generating a test pattern aimed at internal structures such as the memory circuit structure, the memory device structure, layout of memory cells, etc., or by carrying out a partial test in which memory cell blocks are divided.

The algorithmic pattern generation facility (ALPG) of this system can generate such partial test patterns and complicated test patterns aimed at memory internal structures at high speed without dummy cycles.

The ALPG can generate various types of test pattern (N, $N^{3/2}$, N^2, and N^3 patterns) using a microprogram without dummy cycles under microprogram control.

The ALPG has 32 lines of address space: X=16, Y=16
4G words of address patterns can be generated by X and Y addresses alone.

The two (X, Y) address fields can be used to select an address descrambler for conversion between logical and physical addresses, to interchange mutual bits, and to specify nibble address data.

Data patterns can be generated by using two sets of 18-bit test patterns and address functions in the ALPG, or inverting data by address functions.

This ALPG realizes high speed sequence control which can jump, loop, and so on at 133 MHz. There are four pattern generators which generate address/data and are sequence-controlled at maximum 133 MHz. Maximum frequency operation is made possible by the four pattern generators 4 WAY interleave. The maximum frequency is 533 MHz in this system under the 4 WAY mode.

1.2.2 Timing Flexibility

The data clock rate can be set in a range of 1.875 ns to 1.92 μs in 4 WAY interleave, in a range of 3.75 ns to 3.84 μs in 2 WAY interleave and in a range of 7.5 ns to 7.68 μs in 1 WAY operation. The resolution is 14.6484375 ps.

A timing clock between 0 μs and 960 μs can be set with the resolution.

The clock rate and each timing edge can be selected on the fly from previously set 16 levels of the timing set. The strobe for sens and the timing of driver can be set continuously between a certain test cycle to the next cycle (2 cycles - 15.625 ps) in 1 WAY. For 2 WAY, this is available for up to 4 cycles - 14.6484375 ps; for 4 WAY, for up to 8 cycles - 14.6484375 ps. It is the same when the timing is switched on the fly.

Every format channel has two timing clocks used for independent driver waveform. Each timing clock can be used up to 128. Also, every I/O channel has two independent strobe edges and two

timing clocks for I/O control. Two strobe edges can be used for up to 64 channels and two I/O timing clocks can be used for up to 128 channels.

1.2.3 Numerous Waveform Formats

A custom designed pin control register LSI enables the generation of 20 waveforms.

These waveforms fall into four main groups: NRZ, RZ, SBC and FIX. In addition, the system can generate waveform multiplexed within the same cycle.

With its four-point timing calibration function, the driver can calibrate all points.

1.2.4 Logical Comparison

Logical comparison can be performed with the maximum 1.066 GHz by two-strobe edges in 4 WAY interleave.

1.2.5 Unlimited Pattern Selection Functions

The programmable data selector provided for all pins allows unlimited selection of the address, the data and control signals generated by the ALPG.

This enables unrestricted correspondence between test pins and test data, removes limitations on program creation, and improves program productivity.

Unrestricted combinations of multiplexed addresses and data enable a wide variety of device tests.

1.2.6 Test Stations

This system can connect maximum 2 sets of BiCMOS stations which can mount maximum 1344 channels. Simultaneous measurement between stations can be performed in 2 stations configuration.

The minimum pulse width in BiCMOS station is 0.9375 ns / 1.6 V and the accuracy of the minimum amplitude is guaranteed from 0.2 V, which work for the small amplitude high speed interface test.

Features of each channel of the pin electronics include:

- Driver/dual comparator of I/O split construction (I/O CH)
- Dynamic clamp (I/O CH)

1.2.7 DC Parametric Test for Simultaneous Measurement

One station permits installation of up to 32 DC test units which test multiple MUTs simultaneously. This means that DC measuring time for simultaneous measurement is reduced.

Program for parallel testing can be written easily by treating the DC test units as a single unit.

1.2.8 Powerful Failure Analysis System

Under powerful 1.125 G-bit $\times$ 8 (max.) failure memory (option), the fail-bit analysis tool for the MUT cells can display a bit map according to the particular layout of the device cells.

1.2.9 Testing with Auto Handler and Wafer Prober

The test stations are designed so that they can be connected between the wafer prober/auto handler and driver/comparator via the shortest route. The ADVANTEST's unique wafer prober assembly is compatible with major wafer products of other manufacturers and can thus be used without sacrificing speed, waveform quality, and accuracy for both functional and DC parametric tests.

1.2.10 Precision-calibration

For this system, online prescision calibration guarantees ±30 ps driver skew, ±30 ps comparator skew, and an overall timing accuracy of ±100 ps (50% point of 0 to 1.6 V).

The timing is automatically calibrated on a per pin basis during test execution to meet the device structure and test conditions and provide the highest possible accuracy.

The overall timing accuracy includes:

- Clock generator linearity
- Pin-to-pin skew of drivers and comparators
- Clock-to-clock skew
- Format skew, including driver response and waveform symmetry
- Jitter including mutual interference between clock, etc.
- Response ambiguity of comparator
- Response differences between V_{OH} and V_{OL} comparators.

1.2.11 Multi-socket Testing

Table 1-1 shows the number of DR channels and the number of I/O channels to be used for testing one of RDRAM, SDRAM, SRAM, DRAM and other devices in simultaneous measurement mode.

Table 1-1 No. of DR Channels and I/O Channels

1 station configuration	2 stations configuration	DR channel number	DR channel number (For clock generation)	I/O channel number
32	64	18 (–) [–]	3 (–) [–]	24 (–) [–]
16	32	36 (18) [–]	6 (3) [–]	48 (24) [–]
8	16	72 (36) [18]	12 (6) [3]	96 (48) [24]
4	8	72 (72) [36]	12 (12) [6]	96 (96) [48]
2	4	72 (72) [36]	12 (12) [6]	96 (96) [48]

The parenthesized values indicate the number of channels used for the half station configuration.The bracketed values are applied to quarter configuration.

Note: For the half configuration, up to half the devices can be tested simultaneously. For the quarter configuration, up to one fourth of the devices can be tested simultaneously.

1.2.12 Compatibility

This system is designed in consideration of the program upward compatibility with memory test systems such as T5382A, T5365, T5365P, T5591, T5591R, T5585, T5335, T5335P, T5581, T5581H, T5571P, etc.

1.2.13 RASIS (Reliability, Availability, Serviceability, Integrity and Security)

The highest MTBF rate and up-time are achieved by the extremely reliable design and the high level of manufacturing standards.

High serviceability has been achieved by the adoption of the self-diagnostics concept which has taken full interchangeability of boards into consideration from the designing stage. This makes it easy to isolate a faulty board by diagnostic programs. All relays are high-reliability reed relays. Any faulty relay can also be located by diagnostic programs.

- Built-in temperature monitor
- Diagnostic voltage standard
- Diagnostic standard resistors
- Quartz clock oscillator (stability: 1×10^{-5})
- Time and voltage monitor
- Automatic timing correction function
- Self-diagnostic functions

1.3 Compatible Products

This test system belongs to the ADVANTEST VLSI test system family. Wafer prober interface assemblies and auto handlers are also available from ADVANTEST. These compatible products are listed below. For details of each such product, refer to their respective Product Descriptions.

- T3382 100 MHz 512-pin general-purpose VLSI test system
- T3340 series general-purpose VLSI test system
- T3320 series general-purpose VLSI test system
- T5335P 30 MHz 32-memory parallel test system
- T5382A 100 MHz 32-memory parallel test system
- T5365 60 MHz 64-memory parallel test system
- T5365P 60 MHz 32-memory parallel test system
- T5581 200 MHz 64-memory parallel test system
- T5581H 250 MHz 64-memory parallel test system
- T5571P 125 MHz 32-memory parallel test system
- T5591 500 MHz 8-memory parallel test system
- T5585 250 MHz 128-memory parallel test system
- Tester access fixtures for wafer tests and package tests
- ADVANTEST auto handlers

2. TESTER MAINFRAME

This system mainframe consists of the following units:

- High-speed test vector transfer bus and high-speed tester control bus for data transfer
- Algorithmic pattern generator (ALPG)
- Programmable data selector (PDS)
- Timing generator
- Failure analysis memory
- Format control and digital compare
- DC parametric test unit
- Programmable power supplies for devices

Figure 2-1 is a block diagram of the tester mainframe.

2.1 System Buses

This system employs two universal data buses, a tester control freeway and a test vector highway.

The tester control bus is a control signal freeway over which read/write data is transferred between the tester processor and each of the tester mainframe components. The primary functions of the bus are to transfer condition-setting data between various units during functional tests, test conditions for DC parametric testing, and the results of tests.

Since all data, control, and status registers connected to this bus have specific individual addresses, the tester processor can handle the transfer of control information and test patterns as data transfers between memories.

The test vector highway uses coaxial cables to transfer high-quality data, enabling a high-speed functional test.

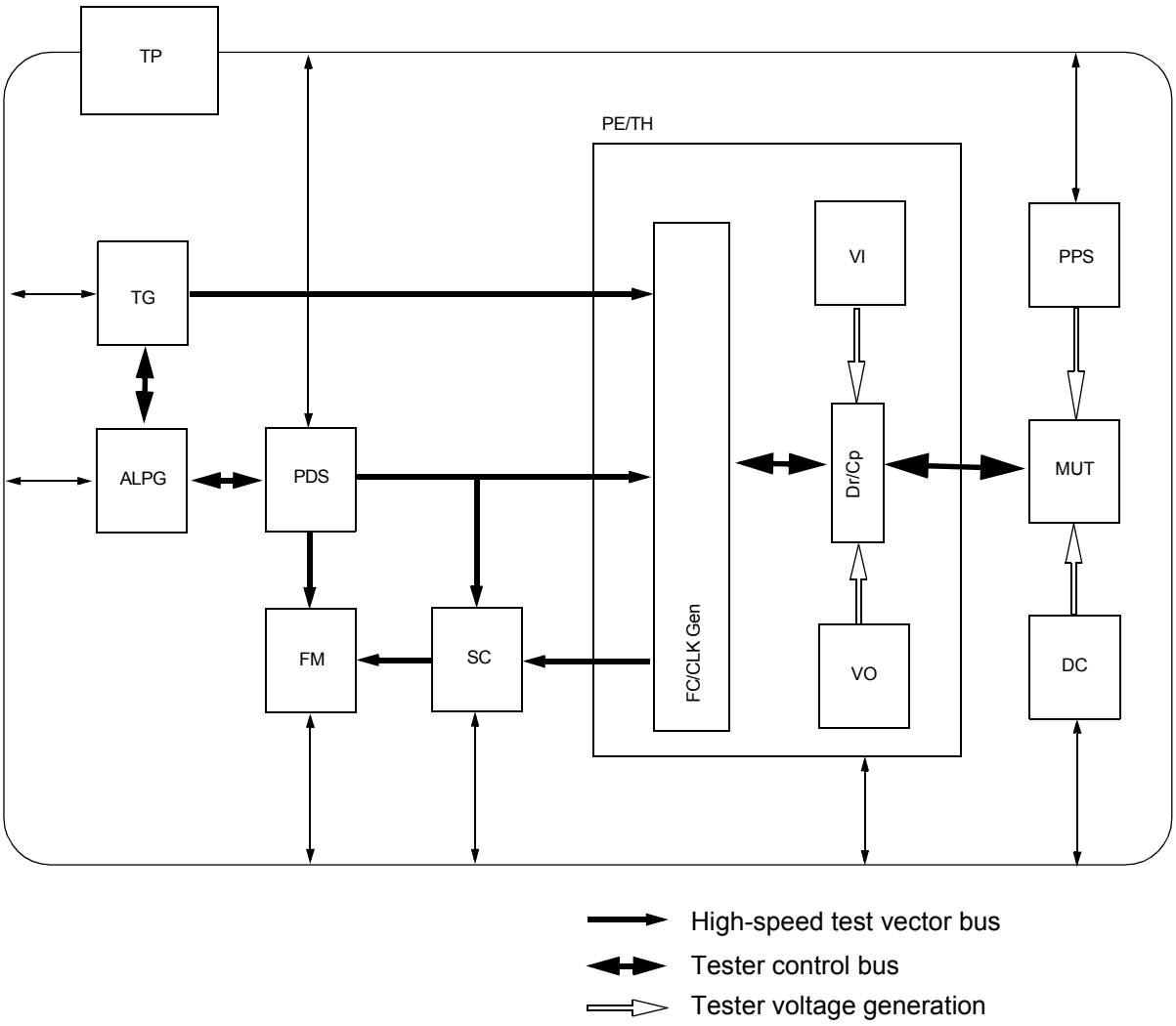


Figure 2-1 Test System Main Frame

TP:	Tester processor
TG:	Timing generator
ALPG:	Pattern generator
PDS:	Data selector
FM:	Failure analysis memory
SC:	Logical comparison
FC/CLK Gen:	Format control or Clock generation
VI/VO:	VI or VO voltage generation
DC:	DC measurement unit
PPS:	Device power supply

2.2 Test Vector Generator

This system test vector generator has the architecture shown in Figure 2-2 which enables it to test efficiently high-capacity, complicated memory devices.

The algorithmic pattern generator (ALPG) generates test vectors for testing memory devices. The programmable data selector unit (PDS) consists of an address descrambler, a pin data multiplexer, and a pin control data multiplexer. It selects the test vector required by the pin electronics unit.

2.2 Test Vector Generator

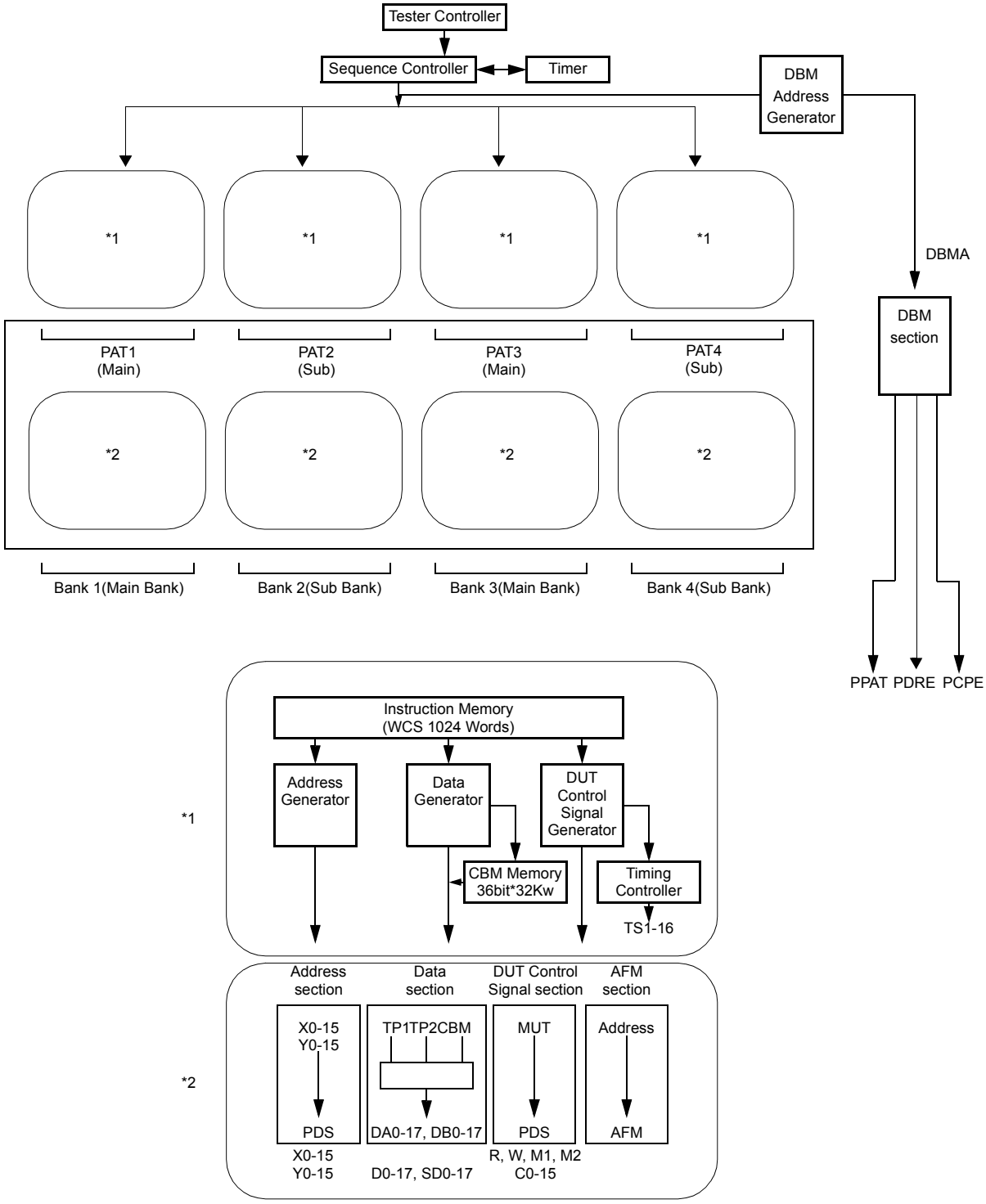


Figure 2-2 Test Vector Generator

2.2.1 Algorithmic Pattern Generator

The algorithmic pattern generator (ALPG) has a ALPG controller and four pattern generators, each of which works at maximum 133 MHz. Pattern generation over 133 MHz becomes possible by specifying 4 WAY interleave mode or 2 WAY interleave mode. These interleave modes allow to generate maximum 533 MHz pattern by describing the same pattern as conventional PCC2 mode.

ALPG controller and the pattern generators consist of the following function blocks.

<ALPG controller>

- Sequence controller
- Instruction memory
- Timing controller
- Tester controller
- Timer

<Pattern generator>

- Address generator
- Data generator
- MUT signal generator
- Timing signal generator

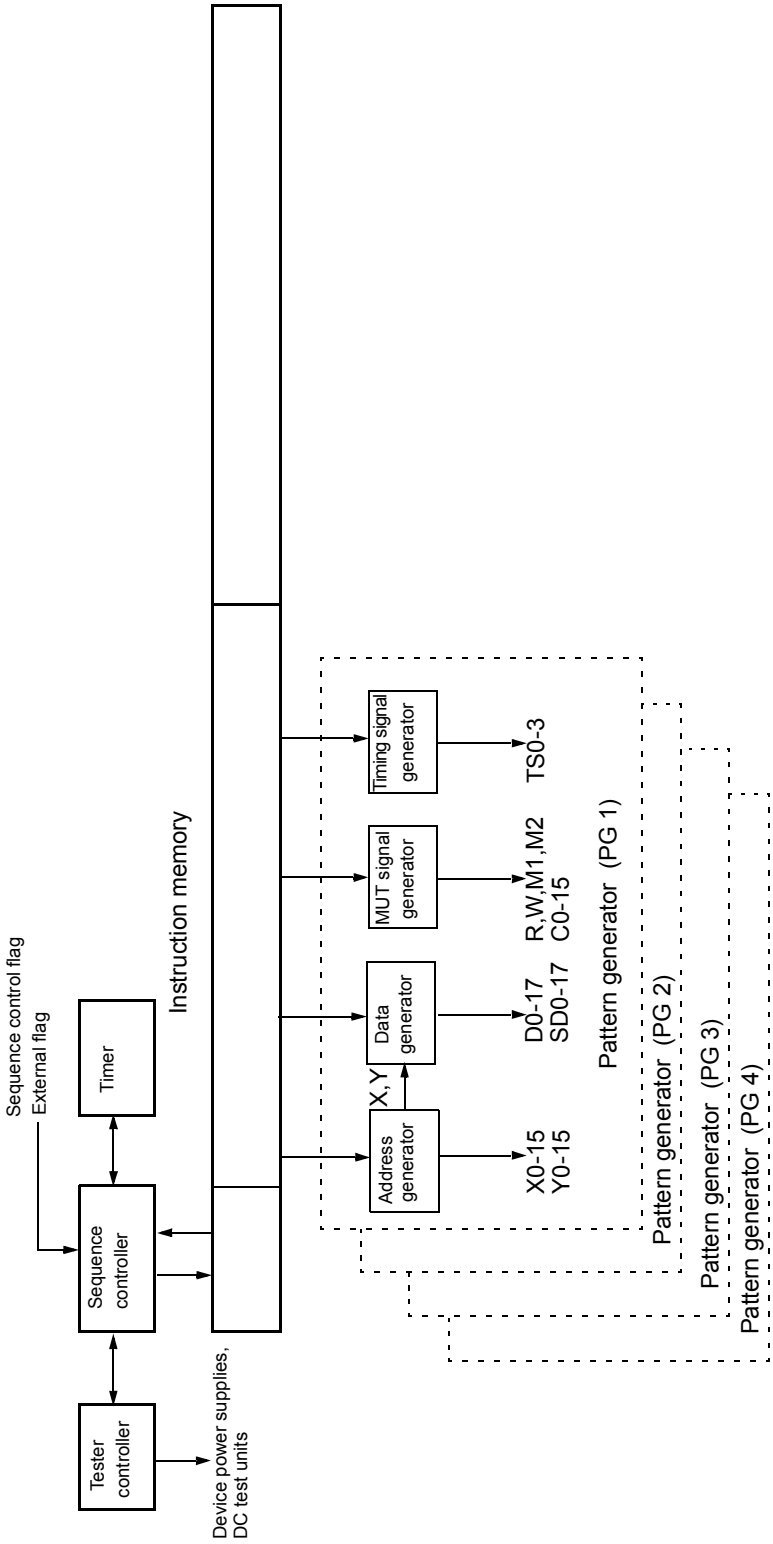


Figure 2-3 Algorithmic Pattern Generator

(1) Sequence Controller/Instruction Memory

The sequence of ALPG controller consists of the registers listed below and an instruction memory, and controls the test pattern generation sequence in accordance with the loop, conditional branch, subroutine jump, flag sense, and other instructions stored within the instruction memory (See Figure 2-4).

WCS	(Instruction memory)	1K-word
PC	(Program counter)	10-bit
STA	(Start address register)	10-bit
ISP	(Interrupt save pointer)	10-bit
BAR	(Branch address register)	10-bit
STK	(Stack register)	10-bit
IDXRn	(n=1-8) (Index register R)	28/24-bit
IDXWn	(n=1-8) (Index register W)	28/24-bit
IDX	(Index register)	24-bit
DFLG	(Data inversion flag)	1-bit
CFLGn	(n=1-8) (Sequence control flag)	1-bit
FLAG	(Matching flag)	1-bit

Index registers 1-2 are 28 bits, and index registers 3-8 are 24 bits.

Loops can be nested up to eight levels, and subroutines can be nested up to four levels. However, if nesting is done by an interrupt, then that nesting operation is not included in the above.

In addition, the SET instruction can be used to set optional data in the address generator and the data generator.

The OUT instruction can be used to change device power setting conditions in synchronization with pattern generation.

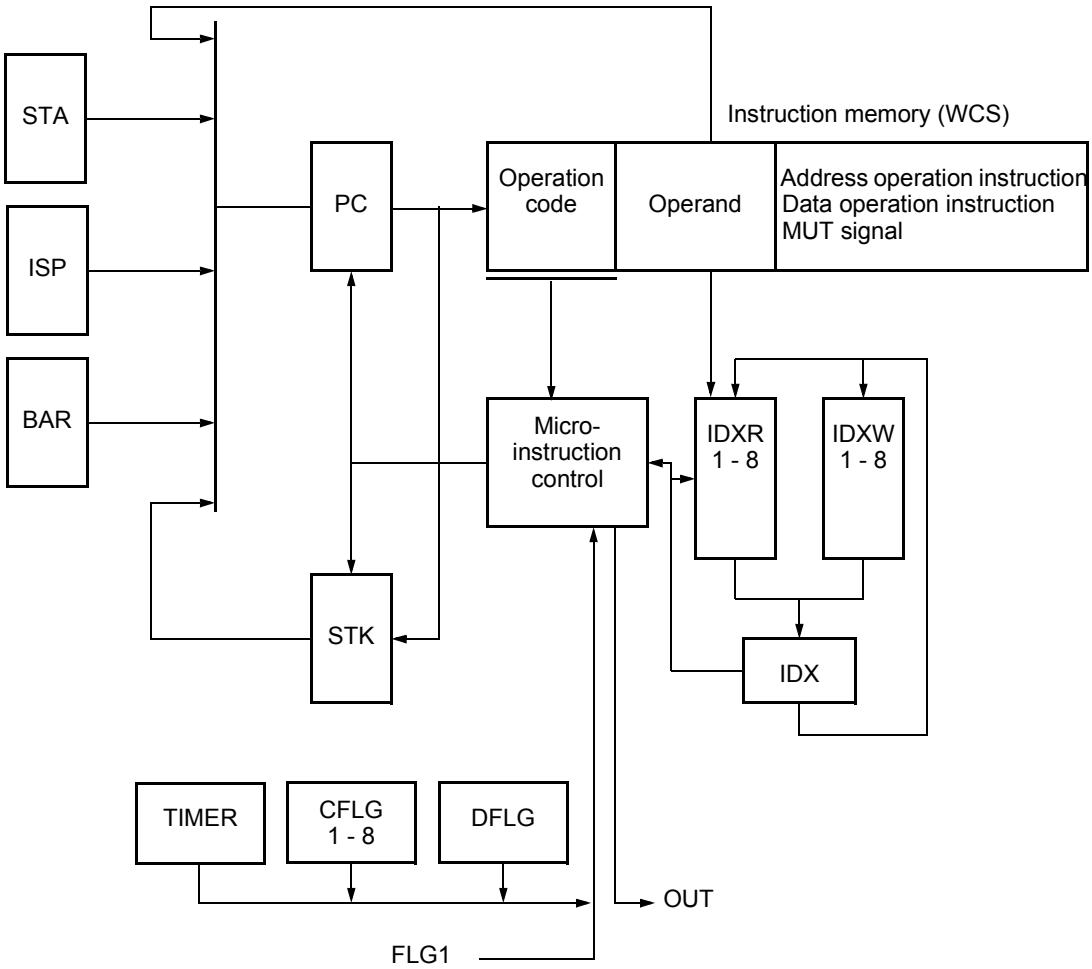


Figure 2-4 Sequence Control Section

(2) Address Generator

The address generator is a part that generates the address patterns to be applied to the MUT in accordance with address operation instructions from the instruction memory. The address generator consists of the registers and the address prescramblers listed below. (See Figure 2-5.)

- X (X address) 16-bit
- Y (Y address) 16-bit
- Z (Partial/Burst address) 16-bit
- N (Nibble/Block address) 4-bit
- RF (Refresh address) 16-bit

The X register and Y register consist of register groups of XH, XB, XC, XS, XK, XOS, XT and YH, YB, YC, YS, YK, YOS, YT, respectively. An X address pattern and a Y address pattern are generated by operations between these registers.

In addition, D1, D2, D3 and D4 register groups are provided as operation registers common to XC, XS, XK and YC, YS, YK. The D3 register can perform increment, decrement, and left shift operations, and the D4 register can perform right shift operations.

The Z register is used to generate block addresses for partial tests and burst addresses of SCRAM.

The N register is used to generate nibble addresses for nibble tests and bank addresses of SDRAM.

The RF register generates the refresh addresses for refresh test. The refresh addresses can be output to X address at regular time intervals previously set on the timer.

Address prescrambler consists of the following function blocks.

- X Pre-SCRAM memory
- Y Pre-SCRAM memory
- XOR-Z
- Adder-Z

X Pre-SCRAM memory and Y Pre-SCRAM memory perform address pattern conversion from X register and Y register with 32K word $\times$ 15 bit memory respectively.

XOR-Z function generates SDRAM interleave burst addresses. XOR got in each bit between the addresses generated in Z register and the addresses from X register and Y register is output.

The adder-Z function generates SDRAM interleave burst address. The addresses generated in Z register and the addresses from X register and Y register are added to be output.

When XOR-Z and Adder-Z functions are used, address bit can be specified for burst length.

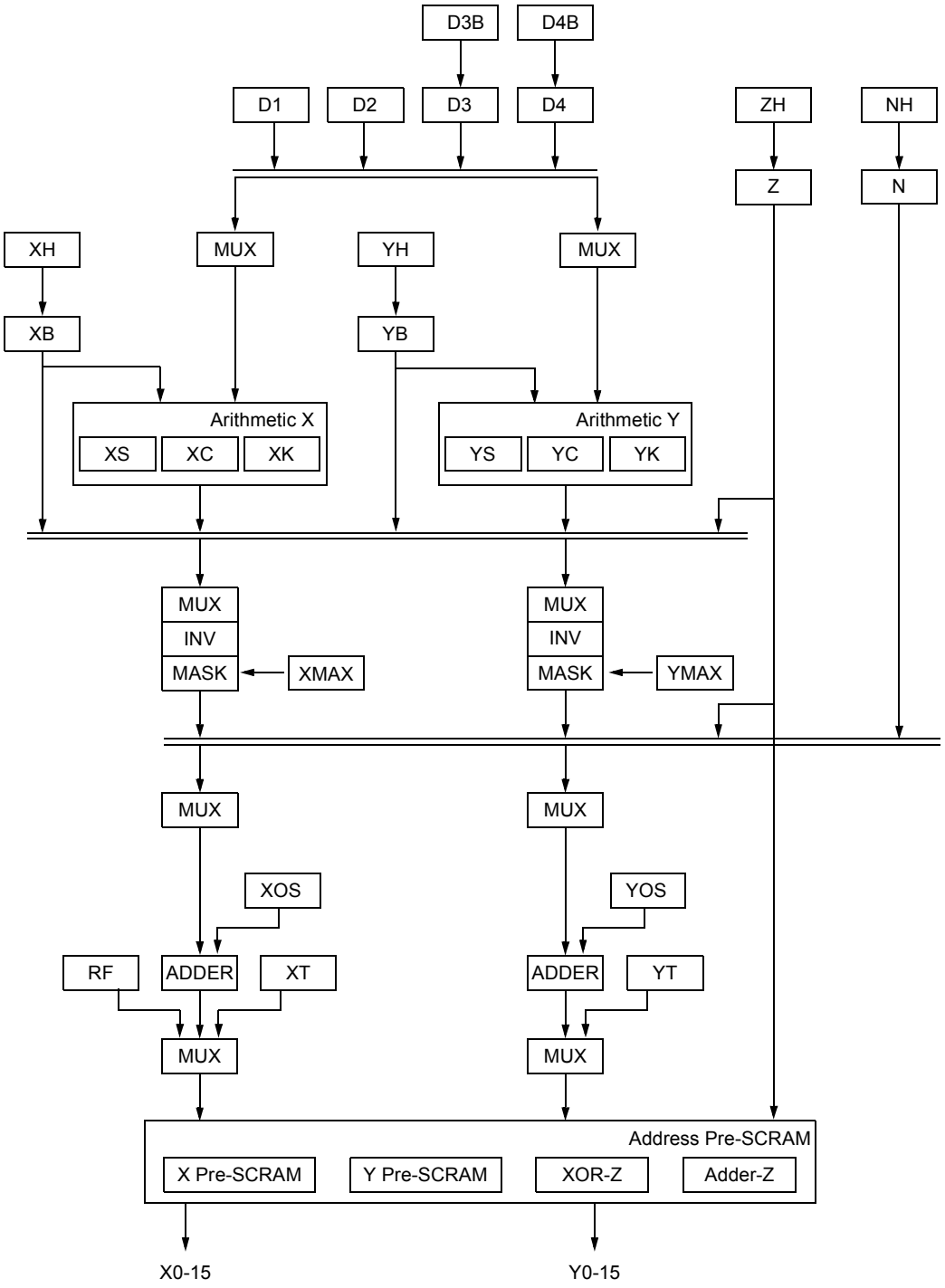


Figure 2-5 Address Generator

(3) Data Generator

The data generator generates the write data and the expected value data which are added to the MUT when an address operation instruction is issued by the instruction memory. The data generator consists of the following registers, area inversion memory, address function data generator, and CBM memory (see Figure 2-6).

- TP1 (Data pattern register 1) 36-bit
- TP2 (Data pattern register 2) 36-bit
- DCMR1 (Data inversion select register 1) 36-bit
- DCMR2 (Data inversion select register 2) 36-bit

TP1 register and TP2 register consist of register groups of TPH1, TPS1, D5 and TPH2, TPS2, D6, respectively. The 36-bit two-system data patterns are generated by performing the computation between these registers.

When data is generated by the data operation instruction, any bit of this data can be inverted in the real-time mode by the data inversion instruction and DCMR1 and DCMR2.

Although data is inverted on both sides of internal sense amp within the DRAM and then charged, the area inversion memory (ARIRAM) can provide free control of the charge around the cell of interest.

The ARIRAM has the 18-bit by 4 KW capacity and it can separately control the inversion of each bit of 18-bit data.

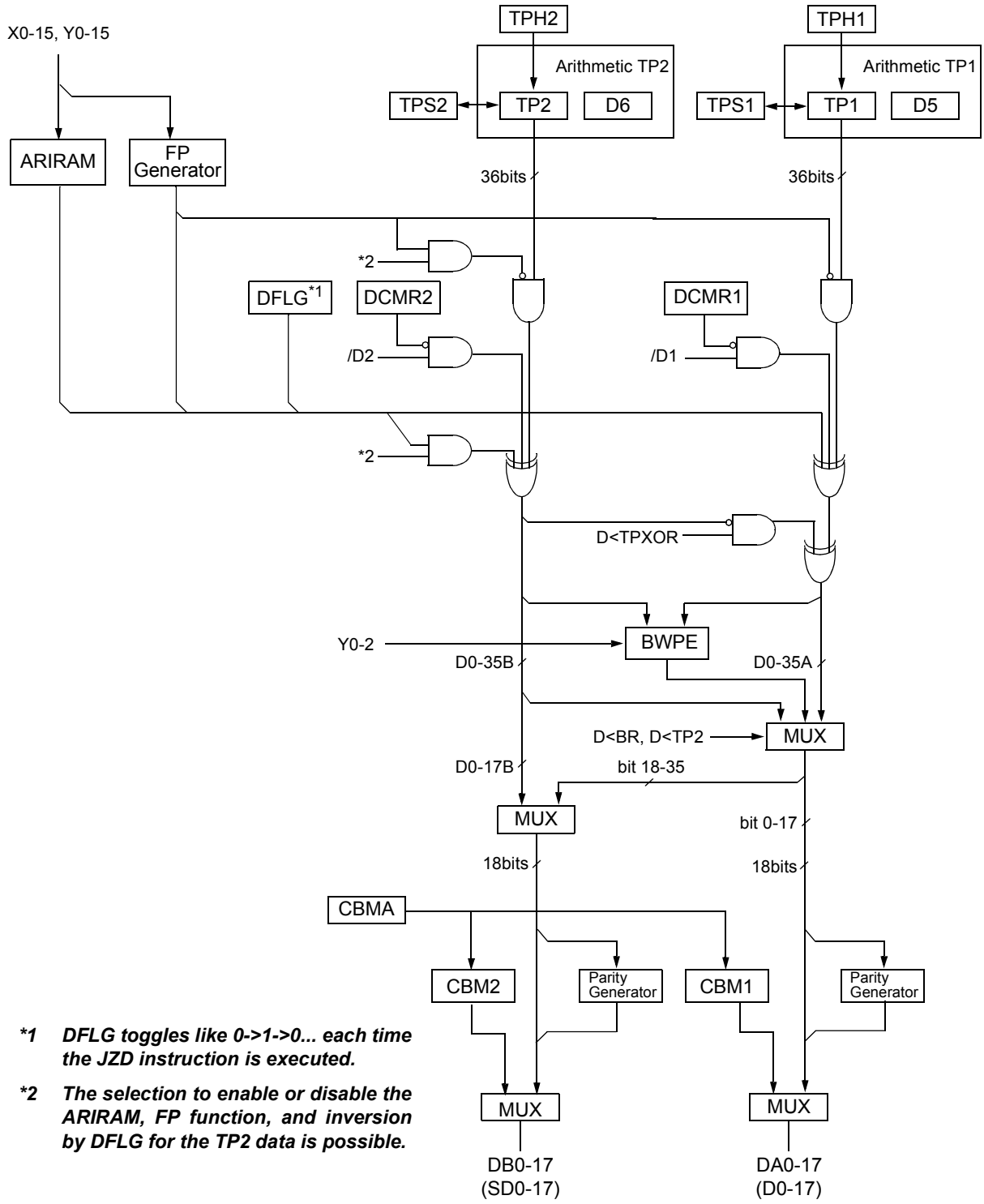
Data that has been generated as address functions (FP) by the X, Y, and Z addresses can be used to invert and then output the contents of TP1 and TP2 registers. The following nine types of address functions are provided:

Fix “0”
Masked Parity
Diagonal
Inverted Diagonal
Masked Diagonal
Masked Diagonal
Masked Row Bar
Masked Column Bar
Checker Board
ANDing between Masked Row Bar and Masked Column Bar

BWPE (Block Write Pseudo Emulator) is the function to pseudo-emulate easily and generate the expected value which is necessary to test SGRAM, etc. having 8 Column $\times$ 8 I/O $\times$ 4 block-write function and is difficult to generate.

The data pattern output from the data generator is 18-bit 2-systems. Therefore, select a mode to output 36-bit data in one system of 36-bit 2-systems data from TP1 and TP2 register or to output the data of 18-bit 2-systems (D0-17 of each register) as the data pattern.

CBM memory consists of two memories, CBM1 and CBM2, which have capacity of 32K word $\times$ 18 bit. The data in CBM2 and CBM2 can be output by switching 18-bit 2-systems data pattern by real-time or mode.



***1** DFLG toggles like 0->1->0... each time the JZD instruction is executed.*

***2** The selection to enable or disable the ARIRAM, FP function, and inversion by DFLG for the TP2 data is possible.*

Figure 2-6 Data Generator

(4) Timing Signal Generator

The timing controller generations one of the 16 test rate/clock delay presetting in real time.

(5) MUT Signal Generator

MUT signal occurrence part occurs of MUT control pattern R, W, M1-2, and C0-15 used for the control signal of the comparison of the signal for the control terminals such as R/W of MUT, CS, and OE and comparators and control signals of turn on/turn off of the driver.

(6) Tester Controller

The tester controller outputs the tester control codes prestored within the instruction memory to the high-speed tester control bus in accordance with the OUT instruction, and then changes the setting conditions for the device power supplies and others.

Use of this function allows bump tests and other tester control operations to be carried out in synchronization with pattern generation.

(7) Timer

The internal timer can be used to carry out pause tests, refreshing tests, and TRAS tests. The setting range of the internal timer is from 100 ns to 409.5 s. Accuracy of each timer setting is shown in ④.

① Pause Test

The cycle that has been specified in the pattern program during selection of the pause test mode prolongs according to the internal timer setting.

② Refreshing Test

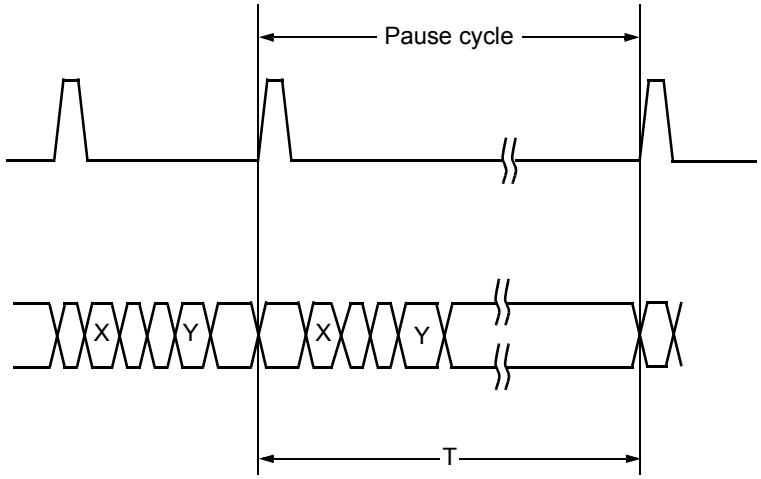
A refreshing test can be conducted using the internal timer and the interrupt function. During selection of the refreshing test mode, the timer first starts operating when the pattern program is specified. When the timer starts to operate, an internal interrupt occurs at the time previously set by the internal timer. Control is automatically branches to the previously specified refresh routine.

③ Branching

When the branching mode is specified, the timer starts operating at the cycle that has been specified in the pattern program. The program counter (PC) branches data into the addresses that have been stored into the interrupt save pointer (ISP) by the timer and signal.

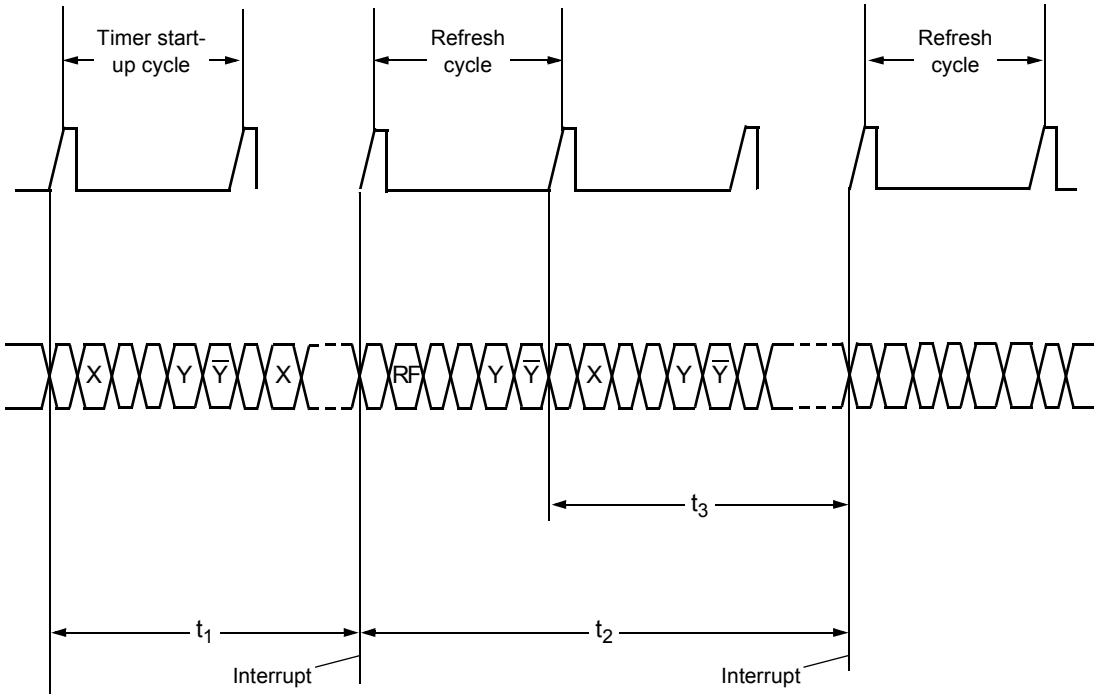
④ Set Accuracy

(a) Pause Test



Run time (T) = (Timer set value + 4 × Timer startup rate + 4.1 μsec) to
(Timer set value + 4 × Timer startup rate + 4.6 μsec)

(b) Refresh Test



			t_1	t_2	t_3
REFRESH A	1WAY mode	Time	Set value +(120 to 146 cycle) +(250 to 350 ns)	Set value +(0 to 13 cycle)	
		Number	Set value +(125 cycle)	Set value	
	2WAY mode	Time	Set value × 2+(240 to 292 cycle) +(250 to 350 ns)	Set value × 2 +(0 to 26 cycle)	
		Number	Set value × 2+(250 cycle)	Set value × 2	
	PCC2 mode	Time	Set value +(120 to 148 cycle) +(250 to 350 ns)	Set value +(0 to 15 cycle)	
		Number	Set value+(125 to 127 cycle)	Set value +(0 to 2 cycle)	
REFRESH B	1WAY mode	Time	Set value+(120 to 146 cycle) +(250 to 350 ns)		Set value+(10 to 36 cycle) +(250 to 350 ns)
		Number	Set value+(125 cycle)		Set value+(15 cycle)
	2WAY mode	Time	Set value × 2+(240 to 292 cycle) +(250 to 350 ns)		Set value × 2+(20 to 72 cycle) +(250 to 350 ns)
		Number	Set value × 2+(250 cycle)		Set value+(30 cycle)
	PCC2 mode	Time	Set value +(120 to 148 cycle) +(250 to 350 ns)		Set value+(10 to 38 cycle) +(250 to 350 ns)
		Number	Set value +(125 to 127 cycle)		Set value+(15 to 17 cycle)

A set value of TIMER can be set in the following range.

TIMER = (time) 200 ns to 409.5 s
or
TREFRESH (number) 2 to 4095

2.2.2 Pattern Memory (DBM)

As a pattern memory, DBM generates a pattern for random logic test.

DBM

DBM consists of four sets of 256 k word(or 1 M word) × 96 bit × 3 data (PPAT, PCPE, PDRE) memories. The relationship between the frequency of the operation and the capacity is as follows. (There is no specification of HS, MS, and LS mode in DBM.)

Operation mode	Maximum frequency of operation	Memory capacity
Normal	~ 133 MHz	256 k word(1 M word) × 96 bit × 3 data
2 WAY	~ 266 MHz	512 k word(2 M word) × 96 bit × 3 data
4 WAY	~ 533 MHz	1 M word(4 M word) × 96 bit × 3 data

2.3 Programmable Data Selector

The programmable data selector consists of the function blocks shown in Figure 2-7.

Address descrambler
Pin data multiplexer
Pin control data multiplexer

- The address descrambler

  Corrects the decoder topology and address topology using the MUT internal structure such as the address decoder, and converts logical addresses into physical addresses.

- The pin data multiplexer

  Selects one of the test patterns generated by the ALPG for each tester pin, so as to match the MUT pin configuration; the test patterns fall into the following two categories:
  Pattern data applied to the MUT by the driver (PATn)
  Expected-value data when outputs from MUTs are logically compared (EXPn)

- The pin control data multiplexer

  Selects tester control signals common to each pin, such as driver on/off control signals and comparator mask control signals.

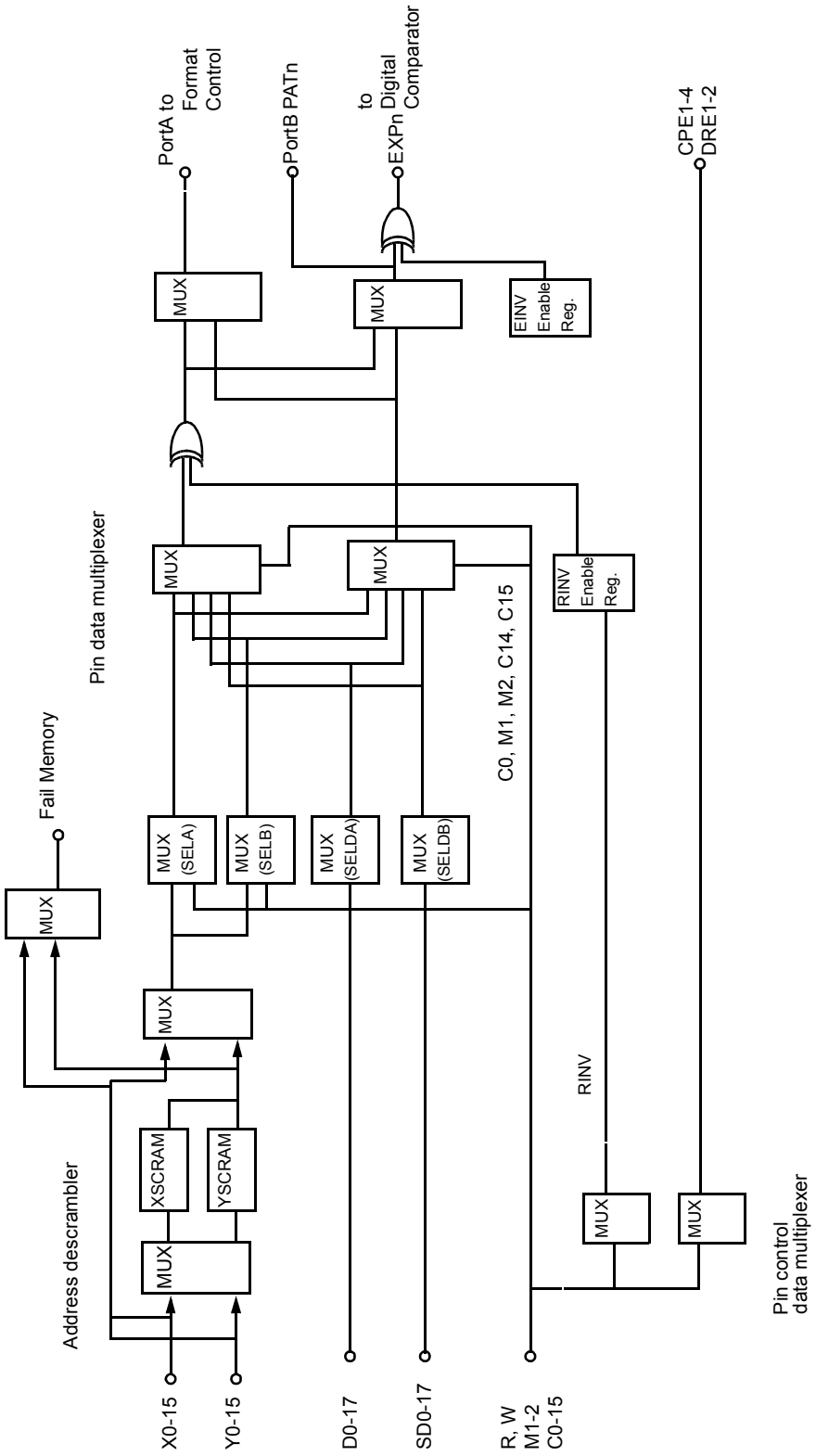


Figure 2-7 Functional Block Diagram of Programmable Data Selector

2.3.1 Address Descrambler

The address descrambler has an address descrambler RAM (SCRAM) which corrects the decoder topology for each of the X and Y addresses, and an address multiplexer which corrects the topology generated between X and Y addresses.

(1) Address Descrambler RAM

The address descrambler RAM consists of the following memories:

- XSCRAM 64K words × 16 bits
- YSCRAM 64K words × 16 bits

(2) Address Multiplexer

The address multiplexer selects addresses applied to XSCRAM and YSCRAM, and each address (X and Y) can be freely selected from among X0 through X15 and Y0 through Y15 respectively.

2.3.2 Pin Data Multiplexer

(1) Pattern data of driver (PATn)

Pattern data can be used all formatter channels consisiting of driver channels(other than channels used for clock generation) and I/O channels.

In the channel specified in RINV enable register, pattern data PATn is inversed at real time by RINV signal selected in the pin control data multiplexer.

PATn is selected from the following SELA, SELB, SELDA, and SELDB.

Each channel has 2 sets of multiplexers which select address signal or MUT signal as SELA and SELB.

2 sets of multiplexers are used to switch 2 patterns on the fly just like ROW address and COLUMN address of address multiplex system.

X0 - 15, Y0 - 15
R, W
M1 - 2
C0 - 15
FIXL, FIXH

Also, each channel has a multiplexer to select D0-17 and SD0-17 as SELDA and SELDB.

C0, M1-2, C14-15 are used as the control signals to switch SELA, SELB, SELDA, and SELDB on the fly.

(2) Expected value data of comparator (EXPn)

It can be used in all I/O formatter channel.

In the channel specified in EINV enable register, the expected value EXPn is inversed.

EXPn is selected from SELA, SELB, SELDA, and SELDB as well as PATn.

2.3.3 Pin Control Data Multiplexer

The pin control data multiplexer selects the following tester control signals common to each pin:

RINV
CPE1 to CPE4
DRE1, DRE2

RINV, CPE1 to CPE4, DRE1 and DRE2 can each select and output the following data:

R
W
M1, M2
C0 to C15
FIXL
FIXH

R, W, M1, M2, C0 to C15 indicate MUT control signals.

(a) RINV

RINV is a signal to control reversing PAT.

PATn is reversed and output by the pin of the RINV enable register whose content is 1, during a cycle when the RINV signal is 1.

(b) CPE1 to CPE4

CPE1-4 are the enable control signals for MUT output test by STRB.

(c) DRE1, DRE2

DRE1 and DRE2 are driver output enable control signals for I/O pins.

2.4 Special Functional Test Modes

This system does not have auto page mode and auto nibble mode functions to switch the timing set automatically by the control signal in ALPG such as address sequence, repeat counter, etc.

This section describes other the special functional test modes of this system.

2.4.1 Direct Tester Control by ALPG

The tester processor reads and writes data to and from each of the hardware units within the tester mainframe over the tester control bus freeway, but this data transfer can also be performed by the ALPG. Synchronized with test pattern generation during the execution of a functional test, data can be transferred in real time from the ALPG to any desired unit, to change the test conditions.

As an example, the execution of a bump test involves the modification of the bias value of the DUT in synchronism with the generation of test patterns. Voltage information concerning the modification can be sent to the device power supply unit. The ALPG is held during the transfer of data from the ALPG to the desired unit.

Figure 2-8 shows the direct tester control provided from the ALPG.

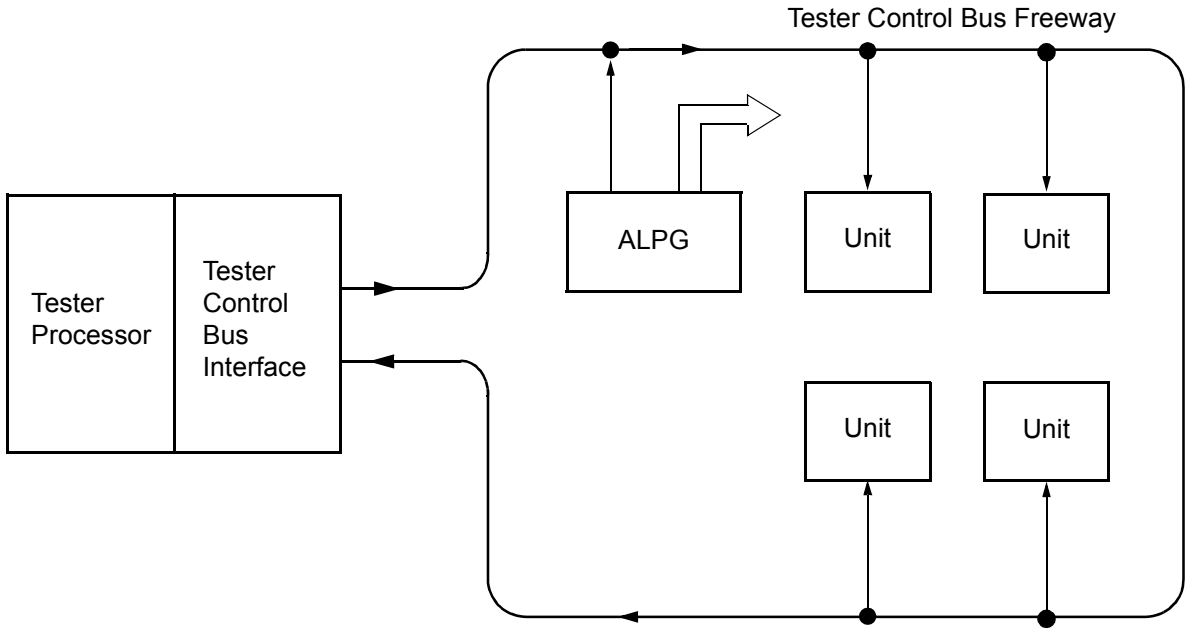


Figure 2-8 Direct Tester Control from ALPG

2.5 Failure Analysis Memory (Optional)

The fault analysis memory consists of an address failure analysis memory unit which analyzes the address at which a failure occurred, and a data memory unit which analyzes the process leading to the generation of the failure.

The address failure analysis memory can generate expected-value data for ROM tests and comparison master data for controlling Care/Don't Care for each bit during memory tests. When several devices are being tested at the same time, several items of device fail information can be fetched simultaneously.

2.5.1 Address Failure Analysis Memory Unit

The address failure analysis memory unit consists of the following memories and registers:

- Fail memory (FM) Optional
- Mark memory 1 k word × 2 bits
- Fail cell counter 31 bits × 9

Four Fail Memory boards/system or eight/system can be mounted.

One Fail Memory board has the capacity of 1 G bits or 4 G bits and maximum 72 ch for fail capturing.

With the multiplexer of the input section, the fail-memories can take the appropriate configuration according to the number of MUT output bits and the number of memory devices to be measured in parallel.

Table 2-1 and Table 2-2 represents the relationship between four factors: (1) the test rate available of 1 G bits; (2) the number of memory devices to be measured in parallel; (3) the number of MUT output bits, and; (4) the fail-memory capacity per MUT.

Table 2-1 Test Rates, Number of Simultaneous Test Devices, Number of Output Bits and Capacity

Condition: 8 FM boards
(1 G bit/board)

Test rate	Number of devices	Number of MUT output bits or FM capacity per MUT					
		1 bit	4 bits	8, 9 bits	16, 18 bits	32, 36 bits	64, 72 bits
1.066 GHz (4way-HS) (double speed)	1	256 MW	64 MW	32 MW	16 MW	8 MW	4MW
	2	128 MW	32 MW	16 MW	8 MW	4 MW	—
	4	64 MW	16 MW	8 MW	4 MW	—	—
	8	—	—	—	—	—	—
	16	—	—	—	—	—	—
	32	—	—	—	—	—	—
533 MHz (4way-HS)	1	512 MW	128 MW	64 MW	32 MW	16 MW	8 MW
	2	256 MW	64 MW	32 MW	16 MW	8 MW	4 MW
	4	128 MW	32 MW	16 MW	8 MW	4 MW	—
	8	64 MW	16 MW	8 MW	4 MW	—	—
	16	—	—	—	—	—	—
	32	—	—	—	—	—	—
266 MHz (2way-HS)	1	1 GW	256 MW	128 MW	64 MW	32 MW	16 MW
	2	512 MW	128 MW	64 MW	32 MW	16 MW	8 MW
	4	256 MW	64 MW	32 MW	16 MW	8 MW	4 MW
	8	128 MW	32 MW	16 MW	8 MW	4 MW	—
	16	64 MW	16 MW	8 MW	4 MW	—	—
	32	—	—	—	—	—	—
133 MHz (1way-HS)	1	2 GW	512 MW	256 MW	128 MW	64 MW	32 MW
	2	1 GW	256 MW	128 MW	64 MW	32 MW	16 MW
	4	512 MW	128 MW	64 MW	32 MW	16 MW	8 MW
	8	256 MW	64 MW	32 MW	16 MW	8 MW	4 MW
	16	128 MW	32 MW	16 MW	8 MW	4 MW	—
	32	64 MW	16 MW	8 MW	4 MW	—	—

Note: ***If eight 4M bit FM boards are installed, the capacity becomes four times higher than the above configuration.***

Table 2-2 Test Rates, Number of Simultaneous Test Devices, Number of Output Bits and Capacity

Condition: 4 FM boards
(1 G bit/board)

Test rate	Number of devices	Number of MUT output bits or FM capacity per MUT					
		1 bit	4 bits	8, 9 bits	16, 18 bits	32, 36 bits	64, 72 bits
1.066 GHz (4way-HS) (double speed)	1	128 MW	32 MW	16 MW	8 MW	4 MW	—
	2	64 MW	16 MW	8 MW	4 MW	—	—
	4	—	—	—	—	—	—
	8	—	—	—	—	—	—
	16	—	—	—	—	—	—
533 MHz (4way-HS)	1	256 MW	64 MW	32 MW	16 MW	8 MW	4 MW
	2	128 MW	32 MW	16 MW	8 MW	4 MW	—
	4	64 MW	16 MW	8 MW	4 MW	—	—
	8	—	—	—	—	—	—
	16	—	—	—	—	—	—
266 MHz (2way-HS)	1	512 MW	128 MW	64 MW	32 MW	16 MW	8 MW
	2	256 MW	64 MW	32 MW	16 MW	8 MW	4 MW
	4	128 MW	32 MW	16 MW	8 MW	4 MW	—
	8	64 MW	16 MW	8 MW	4 MW	—	—
	16	—	—	—	—	—	—
133 MHz (1way-HS)	1	1 GW	256 MW	128 MW	64 MW	32 MW	16 MW
	2	512 MW	128 MW	64 MW	32 MW	16 MW	8 MW
	4	256 MW	64 MW	32 MW	16 MW	8 MW	4 MW
	8	128 MW	32 MW	16 MW	8 MW	4 MW	—
	16	64 MW	16 MW	8 MW	4 MW	—	—

Note: ***If eight 4M bit FM boards are installed, the capacity becomes four times higher than the above configuration.***

The FM operating modes include:

- FAIL fetch
- FAIL fetch when expected value is 0
- FAIL fetch when expected value is 1
- FAIL fetch when MMA of mark memory is 1
- FAIL fetch when MMB of mark memory is 1
- Generating mask pattern of comparison

Each Fail Memory board with 36 ch can be used in different mode. This allows the following:

Each 36-channel Fail Memory board with 36 channels can be used for up to two different modes.

- Separate storage of failure data generated in the test cell and disturb cell
- Separate storage of expected values 0 and 1 failure
- Storage of failure data simultaneously with the generation of comparison mask pattern

The FM can be accessed by either of the addresses before and after that are descrambled by SCRAM. The FM is accessed by addresses specified beforehand from X0 to X15 and Y0 to Y15.

By using the failure counter, the total number of failure times occurring in each row address and column address can be counted.

The fail addresses can also be searched at high speed.

Note: The fail counter operates at 50 ns.

2.5.2 Data Memory Unit

The data failure memory analyzes the process as far as the occurrence of a failure; it consists of the following memory and register:

- Data memory 64 words × 192 bits
- Pattern/fail counter 29 bits

The value in parentheses is valid if the sub-option is added.

The following data is stored in the data memory:

	Main
• Failure address	32 bits
• PC0 to PC9	10 bits
• R (MUT control signal)	1 bit
• W (MUT control signal)	1 bit
• M1, M2 (MUT control signal)	2 bits
• C0 to C15 (MUT control signal)	16 bits
• TS0 to TS3 (timing set selection)	4 bits
• ARIRAM (Area Inversion Memory Output)	18 bits
• D0 to 17, SD0 to 17	36 bits
• Failure data	72 bits

64 patterns of this 192 bits of data are stored under the following conditions:

- 64 patterns immediately preceding any pattern count
- 64 patterns immediately preceding any fail count
- 64 fail patterns generated before any pattern count is reached
- 64 fail patterns generated before any fail count is reached

2.6 Timing Generator

2.6.1 Timing Characteristics

The timing edges generated by the timing generator have the following characteristics.

(a) Multiple timing edges

BCLK and CCLK are used as DR waveform timing edges at all DR pins and IO pins.

DREL and DRET are used as the timing edges of I/O switching at IO pins.

STRB is used as the timing of comparative test at IO pins.

Each of BCLK, CCLK and STRB can be used up to 128. Each of DREL and DRET can be used up to 256.

(b) High setting resolution

The timing resolution of BCLK, CCLK, DREL, DRET and STRB is 14.6484375 ps.

(c) Wide setting range

The timing edge can be set in the range of 0 ns - (2 cycles - resolution) without dead band.

In 4 WAY interleave operation, the setting is possible in the range of 0 ns - (8 cycles - resolution) if the cycle is held constant.

(d) On the fly switching

The test cycles and the timing edges can be selected from 16 timing sets on the fly.

(e) Wide range cycle

The functional test cycle can be set in the range of 1.875 ns to 7.68 μs. The resolution is 14.6484375 ps.

The usages of the timing edges BCLK and CCLK for shaping the driver output waveform are described below.

BCLK is used to determine NRZ waveform change timing, as shown in Figure 2-9.

BCLK and CCLK are used to shape the RZ waveform, as shown in Figure 2-9, with BCLK shaping the leading edge, and CCLK the trailing edge.

BCLK and CCLK are used to provide two types of timing and shape a DNRZ waveform.

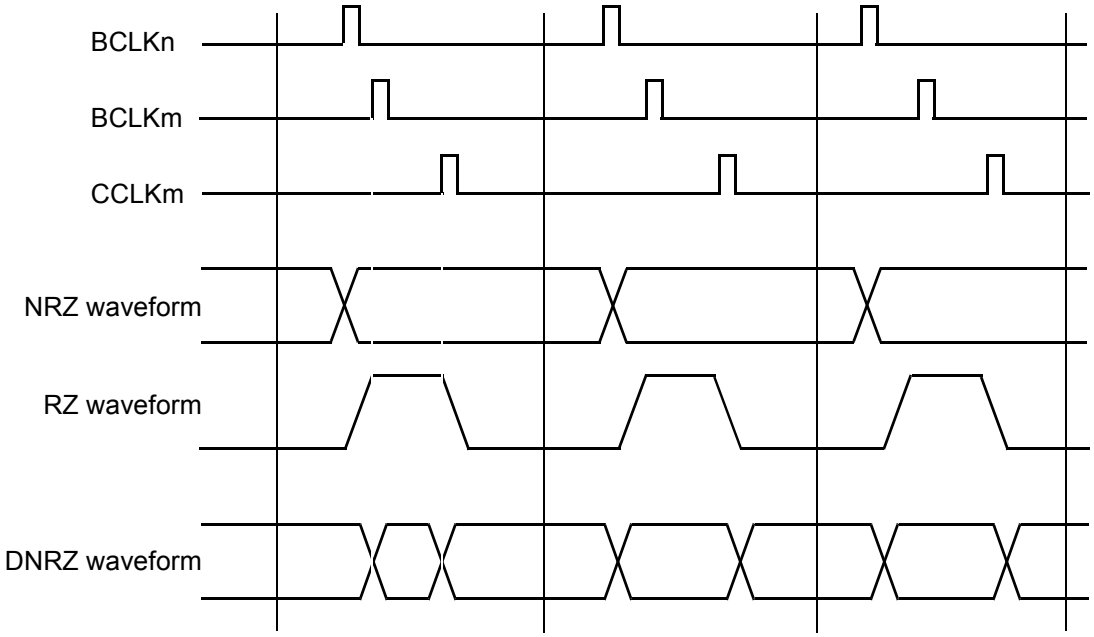


Figure 2-9 Use of Timing Edges

In the 1 WAY operation, as shown in Figure 2-10, a two-phase clock can be output during a single test period. The timing edge intervals are corrected by the autocalibration function. Figure 2-11 shows combinations of timing edges.

In the data selector setting of the pin statement, the pin data A corresponds to CLK(2n-1) and the pin data B corresponds to CLK(2n).

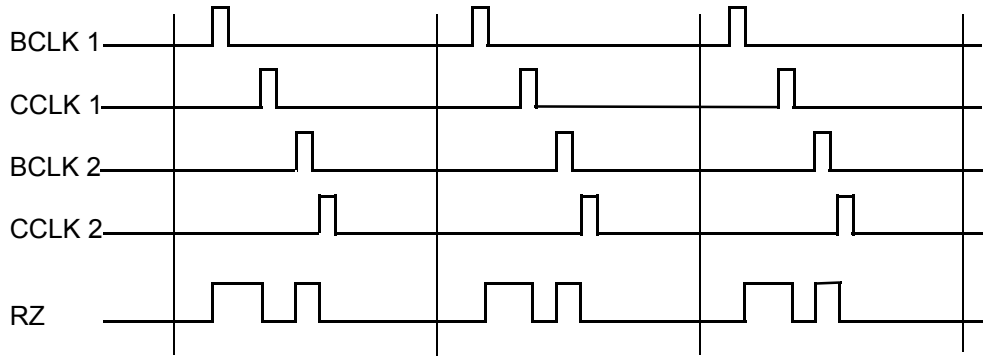


Figure 2-10 Two-phase Clock Output

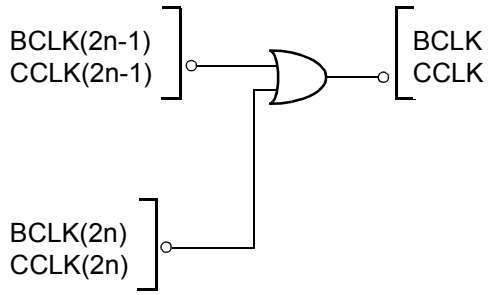


Figure 2-11 Two-phase Clock Output Circuit

DRECLK is used as the I/O selection timing signal to turn on/off the output of the driver in real time, as shown in Figure 2-12.

DRECLK uses one edge (DREL) for the timing of turning the driver on, and one edge (DRET) for the timing of turning the driver off.

To create the DREDNR waveform, two types of DREL and DRET can be set within the test rate.

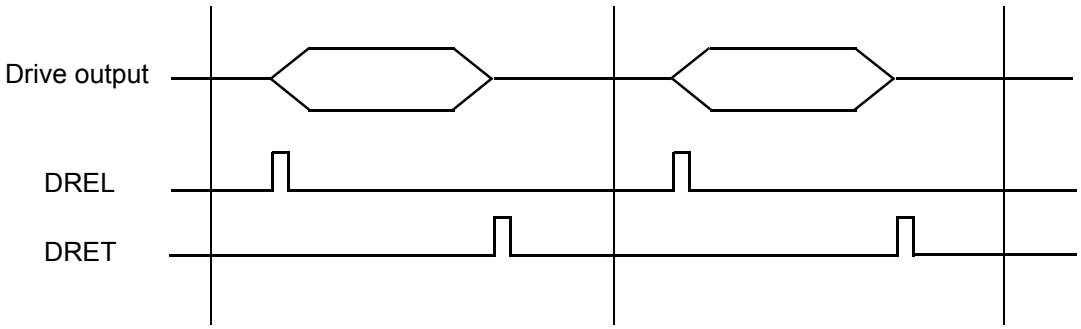
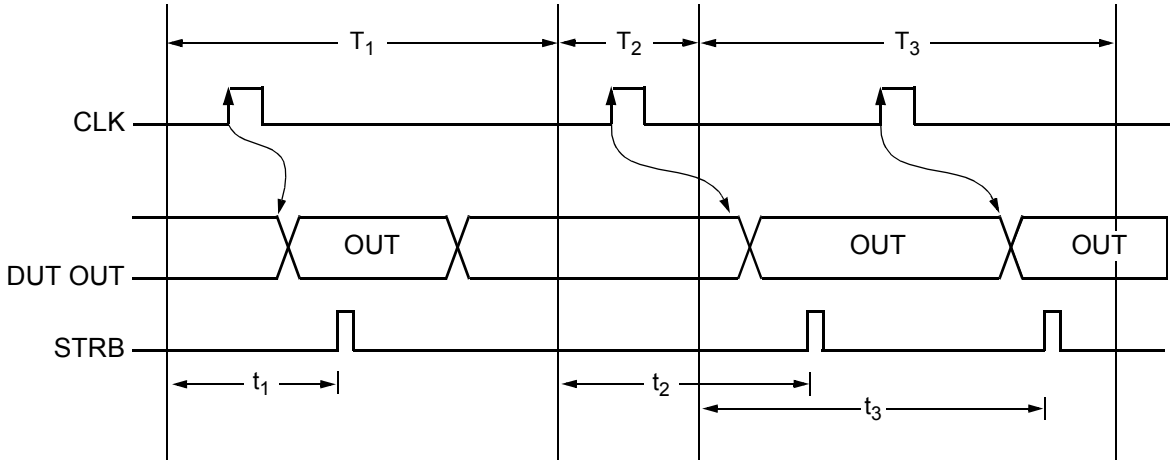


Figure 2-12 Use of DRECLK

During 1 WAY operation, two edge type strobes can be set at each IO pin. When two edge type strobe is set, there is no limitation of space to be set.

Also, during 1 WAY operation, the window strobe can be selected instead of two edge type strobe. The window strobe is used to detect glitch in the specified window.

Figure 2-13 shows the way to switch the strobe without dead band through two test cycles.



T_1, T_2, T_3 : tester cycle
t_1, t_2, t_3 : strobe delay

Figure 2-13 Cross Cycle Strobing

2.6.2 On-the-fly Timing Selection

The timing generator has 16 timing sets, the timing selection can be done on-the-fly by switch control signals TS0 to TS3 from the ALPG. The characteristics of the timing selection are as follows:

- The test period and each of the each of all timing edges, including STRB and DRECK, has 16 values which may be selected on-the-fly.
- There are no restrictions on the 64 timing edges; selection can be done on-the-fly.

2.7 Format Control and Digital Compare

Waveform control is executed based on pattern data generated by the ALPG and selected by the PDS.

2.7.1 Format Control

A waveform is determined by a selection of pattern data and the timing edges of BCLK and CCLK.

Each pin can generate the waveform shown in Figure 2-14. These waveforms can be classified into four basic groups: NRZ, RZ, SBC, and FIX. The timing of each waveform can be done the precision calibration.

By specifying multiplex mode, using the PDS to select two data values for PATA and PATB, two multiplexed waveforms can be output within the same test cycle. This is used to test memories provided with a address multiplex function.

Multiplex waveforms can be generated in all of the 20 waveform modes.

Multiplex mode (SDM) to output two patterns in the same cycle can not be performed in this system.

But if PATA and PATB are switched to real time one by one pattern with the synchronous memory, it can be used with each WAYs without interleave limitation.

DNRZ and /DNRZ modes to output two NRZ waveforms are provided in the same cycle. These modes are used to output patterns of PATA and PATB each in the timings of BCLK and CCLK. DNRZ and /DNRZ can be used in either of each WAYs modes.

CLOCK OPEN can be used for the real time switching of driver waveform without the limitation of waveform mode. Therefore, it is not necessary to edge-inhibit by ALPG pattern or control the real time waveform mode for switching the address waveform between SBC and NRZ, for instance.

Channel number of the format control (FC) to generate independent waveform can be selected by specifying a system type. FC channel number depends on Full/Half or Quarter configuration of the test station.

FC channel number	Full/Half configuration	Quarter configuration
Driver channel	72	36
I/O channel	96	48

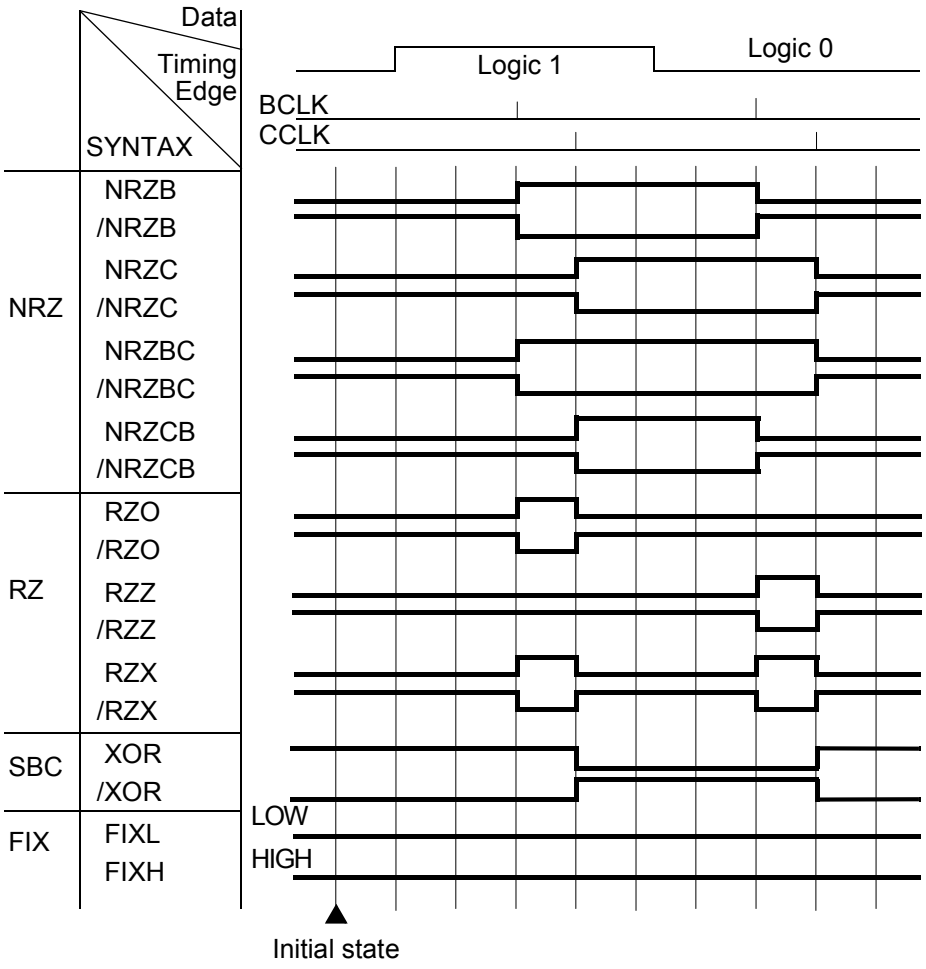


Figure 2-14 Waveform Formatting

2.7.2 I/O Control

I/O control of the driver is determined by using DRE1, DRE2 selected by the PDS.

I/O changeover timing is determined by DRECLK generated by the timing generator. As shown in Figure 2-15, the leading edge of DRECLKL establishes the off-to-on timing of both the RZ and NRZ waveforms, and the leading edge of DRECLKT establishes the on-to-off timing.

2.7.3 Digital Compare

The digital compare logically compares MUT outputs with expected-value data of each pin selected by the PDS.

The comparison is controlled by CPE1-14 signal generated by ALPG and selected at each strobe at each pin.

During 1WAY operation, two edge type strobes can be set at each IO pin regardless of the interleave mode setting. Two strobes can be set in one cycle to compare and test with two timings. In this case, this case, the expected value can be switched for 2 strobes. The window strobe can not be used in this system.

Hi-Z comparison can be set in pin unit without strobe limitation, and H/L comparison and Hi-Z comparison can be performed in the same cycle simultaneously.

It is impossible to set OPEN the strobe irrespective of the mode of 1 WAY, 2 WAY or 4 WAY.

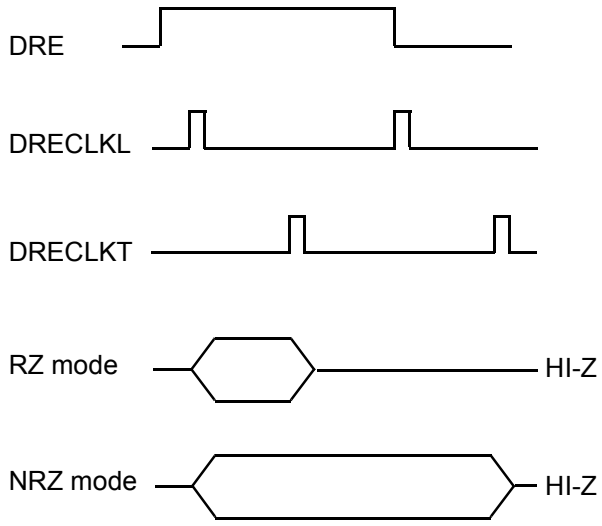


Figure 2-15 Driver I/O Control

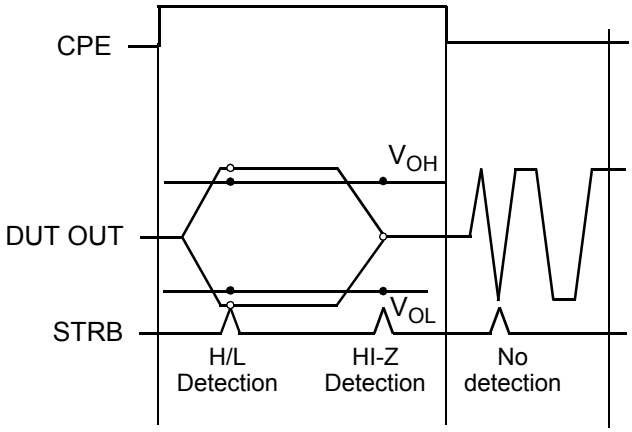


Figure 2-16 Digital Compare

2.8 Test Stations

This system permits connection of up to two units of BiCMOS station which can install maximum 1440 CH.

2.8.1 Pin Electronics

Each pin on a pin card consists of a driver and a dual comparator.

The pin electronics include a driver pin electronics on which only drivers are mounted and an I/O pin electronics on which drivers, comparators and dynamic load switch are mounted.

(1) Driver Pin Electronics

The drive is divided into a lamp generation unit and a buffer unit, output amplitudes from 0.2 Vp-p to 8.0 Vp-p can be output. However, these amplitudes are not guaranteed.

The minimum pulse width of driver 0.9375 ns is guaranteed under amplitude 1.6 Vp-p.

The rise and fall times are 400 ps ± 100 ps / 1.6 Vp-p (20% to 80%).

The combination of output levels V_{IH} and V_{IL} can be selected from up to 16 types by a program. Output impedance is 50 Ω ± 5 Ω.

A block diagram of the driver pin electronics is shown in Figure 2-17.

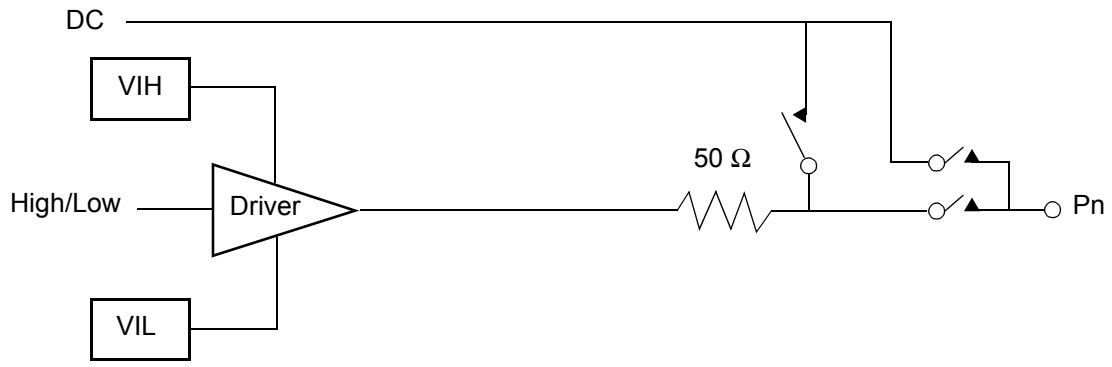


Figure 2-17 Driver Pin Electronics of BiCMOS Station

(2) I/O Pin Electronics

Each driver has the same performance as the driver-dedicated pin electronics. Each dual comparator uses independently programmable V_{OH} and V_{OL} as reference levels. The results of level determination are sent to the digital compare unit for logical comparison based on a strobe timing. There are 16 possible reference pairs of V_{OH} and V_{OL} which can be selected under program control. The input range of the comparators is -2.5 V to 5.5 V. In some cases, it could be desirable to have the output terminated by a resistor, depending upon the device. This can be achieved by applying 50 Ω to the programmable V_{TT}.

The programmable loading can not be used in this system.

The dynamic clamp clamps, at the preset level, the overshoot due to mismatching between the transmission line impedance and device-output signal and absorbs the overshoot to decrease the ringing for correct judgment by the comparator.

The block diagram of the I/O pin electronics is shown in Figure 2-18.

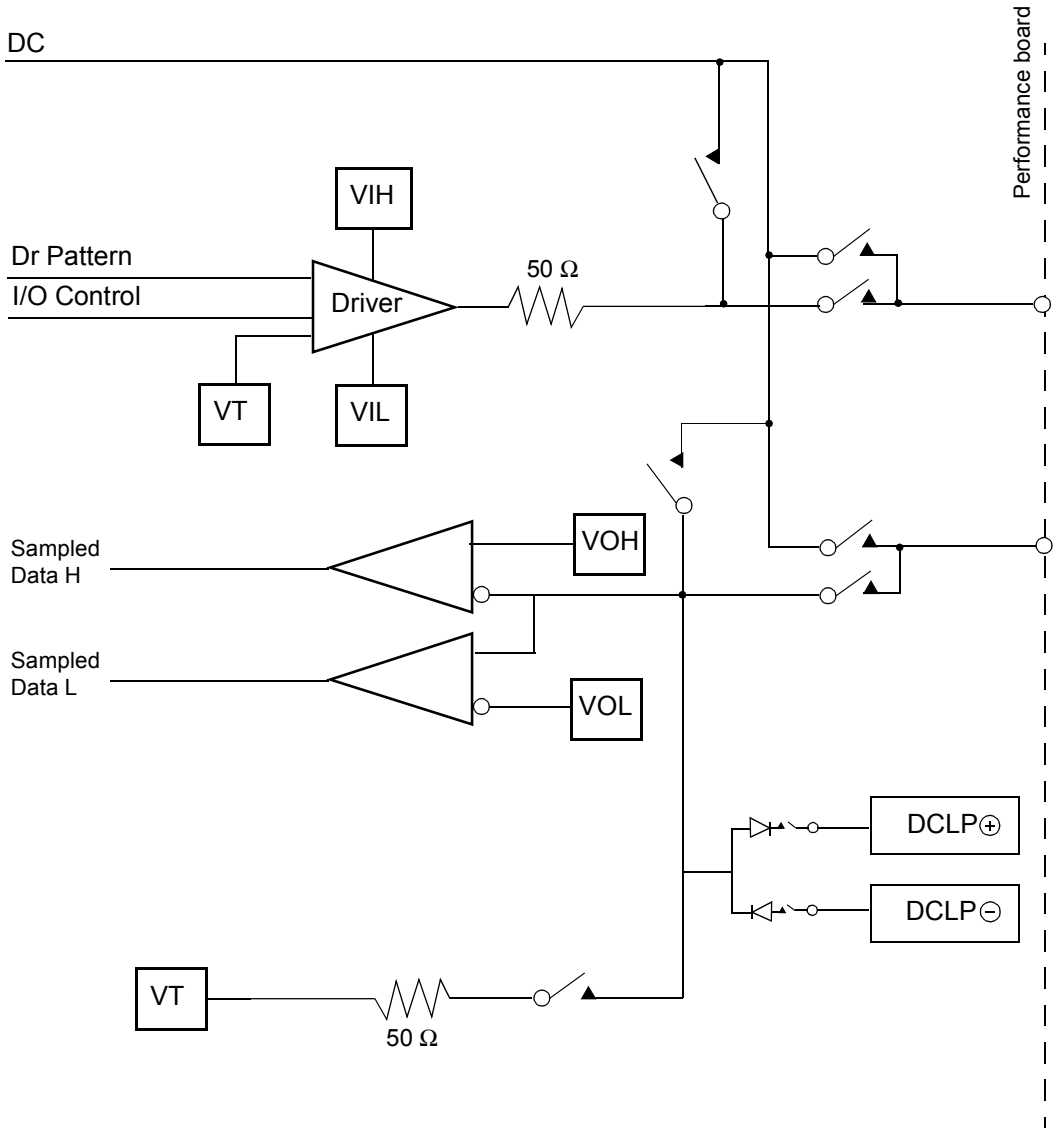


Figure 2-18 I/O Pin Electronics for BiCMOS Station

2.8.2 Test Head Channel Configuration

BiCMOS station pin configuration

The following types of pin configurations can be selected according to the number of DR channels and I/O channels. Two stations in a system should have the same pin configuration.

Test station pin configuration	Full	Half	Quarter
Driver channel	576	288	144
Driver channel (For clock generation)	96	48	24
I/O channel	768	384	192

Childs A, B, C, D, E, F, G and H are available for the full configuration. Childs A, B, C and D are availabe for both the half and quarter configurations.

For the half configuration, up to half the control channels can be used.
For the quarter configuration, up to one fourth of the control channels can be used.

(1) Full/Half Configuration

(a) 18DR+3CLKDR+24IO

DR pin

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
A						DUT1			DC1										CLK_DR		
	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85
A						DUT2			DC17	(DC1)									CLK_DR		
	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149
A						DUT3			DC2										CLK_DR		
	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213
A						DUT4			DC18	(DC2)									CLK_DR		

IO pin

	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56
A		DUT1		DC1																				
	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120
A		DUT2		DC17	(DC1)																			
	161	162	163	164	165	166	167	168	169	170	171	172	173	14	175	176	177	178	179	180	181	182	183	184
A		DUT3		DC2																				
	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240	241	242	243	244	245	246	247	248
A		DUT4		DC18	(DC2)																			

(b) 36DR+6CLKDR+48IQ

DR pin

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
A						DUT1			DC1										CLK_DR		
	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85
A						DUT1			DC1										CLK_DR		
	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149
A						DUT2			DC2										CLK_DR		
	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213
A						DUT2			DC2										CLK_DR		

IO pin

	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56
A		DUT1		DC1																				
	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120
A		DUT1		DC1																				
	161	162	163	164	165	166	167	168	169	170	171	172	173	14	175	176	177	178	179	180	181	182	183	184
A		DUT2		DC2																				
	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240	241	242	243	244	245	246	247	248
A		DUT2		DC2																				

2.8 Test Stations

(c) 72DR+12CLKDR+96IQ

DR pin

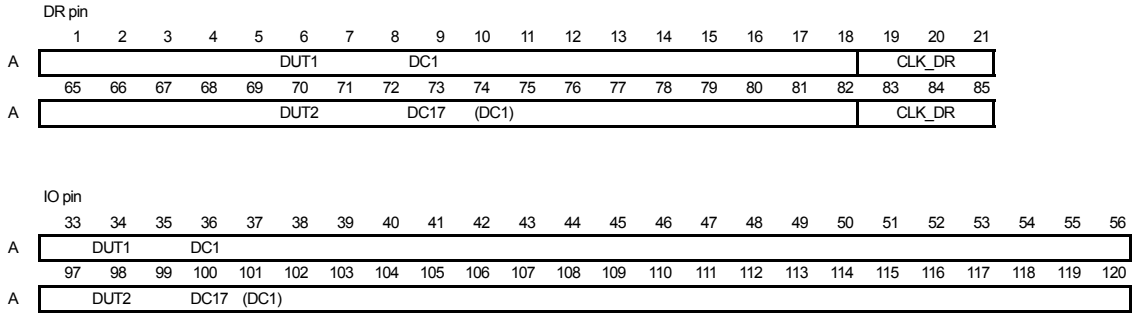
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
A						DUT1			DC1										CLK_DR		
	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85
A						DUT1			DC1										CLK_DR		
	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149
A						DUT1			DC1										CLK_DR		
	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213
A						DUT1			DC1										CLK_DR		

IO pin

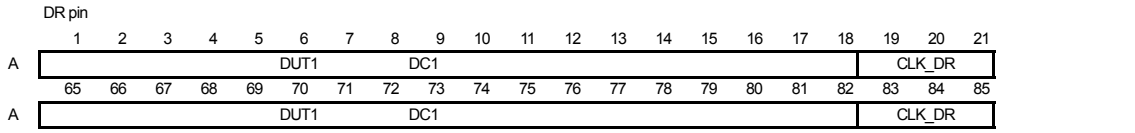
	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56
A		DUT1		DC1																				
	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120
A		DUT1		DC1																				
	161	162	163	164	165	166	167	168	169	170	171	172	173	14	175	176	177	178	179	180	181	182	183	184
A		DUT1		DC1																				
	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240	241	242	243	244	245	246	247	248
A		DUT1		DC1																				

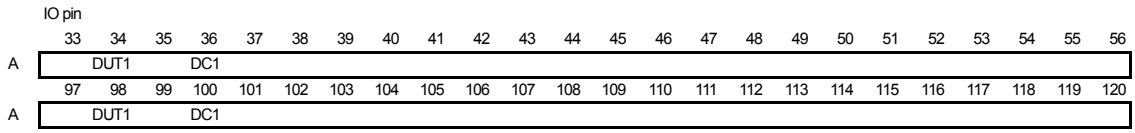
(2) Quarter Configuration

(a) 18DR+3CLKDR+24IQ



(b) 36DR+6CLKDR+48IQ





2.9 DC Parametric Testing

In this test, voltage is applied to a device (MUT) to measure the current flowing through it, or current is fed to MUT to measure the voltage generated across it.

Multiple DC test units mounted to this system permit DC parametric test to be executed simultaneously when connected to the pins used for simultaneous measurement.

Usually, one unit of DC is allocated to one MUT. If the number of MUTs is larger than the number of DCs, one DC is allocated to two MUTs, and measurement is performed by automatically switching DC connection.

When creating a simultaneous measurement program using DC test unit, the program can be described as a measurement program for one MUT.

Each DC test unit incorporates a comparator for determining GO/NO GO, and this results in a reduced testing time.

The voltage range is from -6 V to +10 V, and the current range is ±80 mA.

Very small current can be measured using the ±8 μA (full scale) range.

Each station permits mounting of up to 32 DC test units.

2.10 Device Power Supply

Each station permits incorporation of up to 128 units of power supply for feeding bias voltage to the MUTs.

Eight values for each voltage and current clamp are settable by programming and either of eight set values can be selected in each power supply.

When multiple-device parallel-measurement program is created, the same value is automatically specified by the program to the power supply connected to the same power supply pins of the MUTs.

In the range of output voltage from -6 V to +16 V, the output current is max. 400 mA, and in the range of 0 V to +5 V, the output current is max 800 mA.

All the power supplies have current measurement function.

2.11 MUT Interface

2.11.1 Manual Test Performance Board

To manually test a MUT, a MUT socket is attached to the performance board provided by Advantest Corporation. Assemble the performance boards by wiring each socket pin to an output of the test head pin electronics.

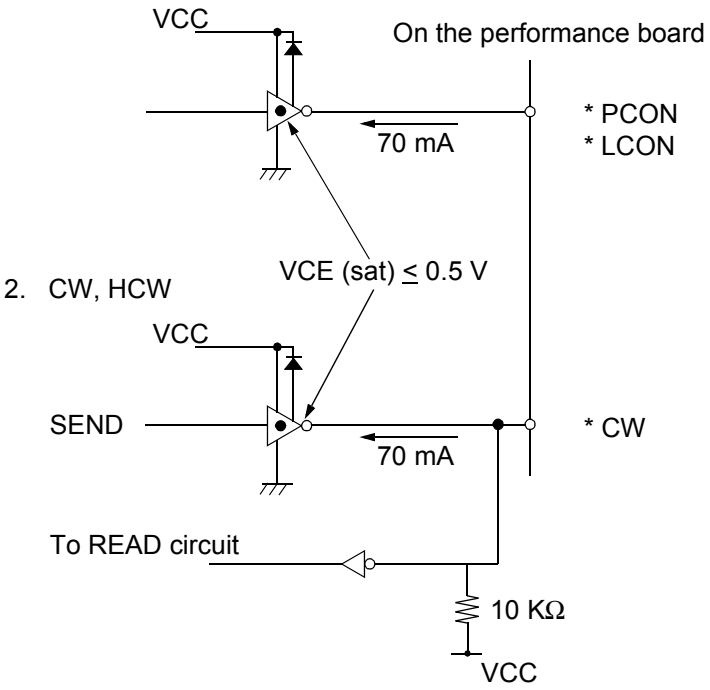
The main I/O signal terminals of the performance board, and their uses, are shown in Table 2-3.

Table 2-3 Terminals on Performance Board

Type	Usage
PIN	Outputs of test head pin electronics. The DUT socket pins are wired to these points.
CW	32 I/O terminals for control words. Used to output signals from these terminals as required by the test program, and branch the sequence under program control by reading the level of these terminals. Used to control circuits mounted on the performance board.
MCW	32 I/O terminals for the expanding control words. These signals can be set and read independently on 2 test heads.
Device power supply output	Output points for device power supplies. These points are wired to the DUT power supplies.
Utility power supply	+5 V is output. This output voltage can be used on the performance board as required. (10 A max. at +5 V)
PCON	Control signal of relay for connecting/disconnecting by-pass capacitor.
LCON	Control signal of relay for connecting/disconnecting load.

Equivalent circuit

1. PCON, LCON



Performance boards and associated accessories are available on request after purchase of this system.

2.11.2 Handler Test

The auto handlers manufactured by ADVANTEST are designed to allow for connection to this system, so that a highly accurate total system containing the tester and handler can be configured.

2.12 Autocalibration System

This system has a built-in autocalibration system which calibrates automatically under the control of the system software. High test reliability and accuracy can be obtained because the system corrects not only timing accuracy, but also voltage and current accuracy.

The calibration performed by this system is broadly classified into two areas: test program independent and test program dependent autocalibration.

In both timing and analog calibrations, hardware multiplexing and reference values are used, and any detected errors are sent to a correction circuit to provide calibration. All channels of the test head pin electronics are connected to a reference comparator. The DC parametric test is used to calibrate the DC level of each pin. The timing of each pin is calibrated with a delay vernier circuit.

Errors specific to individual pins, e.g., clock skew or waveform errors, are calibrated out by the autocalibration system.
Simply stated, the calibration system in this system is much more than a deskew circuit.

2.12.1 Test Program Independent Autocalibration

This calibration corrects any errors inherent to the system which are independent of the test conditions set for the test program. Thirty minutes after power is turned on, the system software activates the calibration program automatically.

The following start-up calibrations are performed:

- Linearity of all edges output by timing generator
- Driver output level offset
- Comparator reference level offset

2.12.2 Test Program Dependent Autocalibration

A test dependent calibration is done based on the test program conditions. Since the test conditions normally change several times during a test, calibration is performed with each change.

The items calibrated under the test program dependent autocalibration are:

- Driver pin-to-pin skew
- Comparator pin-to-pin skew
- Skew between driver and comparator
- Driver I/O timing.

The calibration is provided for only those pins actually used in the test, but when the test conditions relating to these pins change, the pins affected by the new conditions are calibrated.

For more information, refer to “T5500 Series Memory Test System Precision Calibration Program Reference Manual.”

2.12.3 Overall Timing Accuracy

For this system, the term “overall timing accuracy” means the system timing accuracy. In general, when a result of a MUT measurement is A, the accuracy of A is given by A $\pm\alpha$. (α is a fixed value for each system.)

α for driver accuracy includes driver skew, linearity of output clocks, clock-to-clock skew, format-to-format skew, and jitter.
For a comparator, it includes the linearity of the strobe, pin-to-pin skew, skew between dual comparators, driver-to-comparator skew, and timing errors.

The overall timing accuracy of this system is $\pm$100 ps. These overall timing accuracy are guaranteed by autocalibration in the status of 0 to 1.6 V, 50% which includes all above important factors.

2.13 Safety Interlocks

Various types of safety interlocks are provided in this system to ensure safety for the system.

2.13.1 Temperature Alarm Detector

Both the mainframe and the test head are fitted with thermal sensors.
When these sensors detect abnormal temperature, the main power supply is automatically turned off and an alarm message is displayed on the VKT if the test processor and environment processor can communicate with each other.

2.13.2 Power Failure Detector

If an abnormal output of the DC power supply used in the system is detected, then the main power is automatically turned off and an alarm message is displayed on the VKT, as in the case above.

2.13.3 Smoke Alarm Detector

A smoke detector is provided to detect unusual smoke in the mainframe. If smoke is detected by the ion-type smoke sensors installed on the top of the mainframe, then the main power is automatically turned off and an alarm message is displayed on the VKT.

2.13.4 EMO Switch

The EMO switch is used to turn off the system power in cases of emergencies such as the occurrence of an abnormality in the installation location of the system. One EMO switch is provided as standard, and if necessary, another switch can be added as an option.
The following three types of EMO switches are available:

(1) EMO Switch Without a Key (without the guard)

This EMO switch is standard and is not guarded against inadvertent or unauthorized depression of the switch.

(2) EMO Switch Without a Key (with the guard)

This EMO switch is guarded against inadvertent or unauthorized depression of the switch.

(3) EMO Switch with a Key

This EMO switch does not permit power to be turned back on, once it has been turned off in an emergency, until the emergent state is cleared using the switch key.

2.13.5 Fan Stop Detection

All fans have a fan stop sensor in the mainframe.

When a fan stops, the main circuit breaker automatically switches off and a message is displayed on the video keyboard terminal (VKT).

3. COMPUTING

This chapter describes in detail the functions of computing system of the System.

3.1 Computing System

Figure 3-1 illustrates the basic components of the computing system for the System. The computing system is composed of the dual processor, peripheral devices and programming stations, and an interface to communicate with an external network.

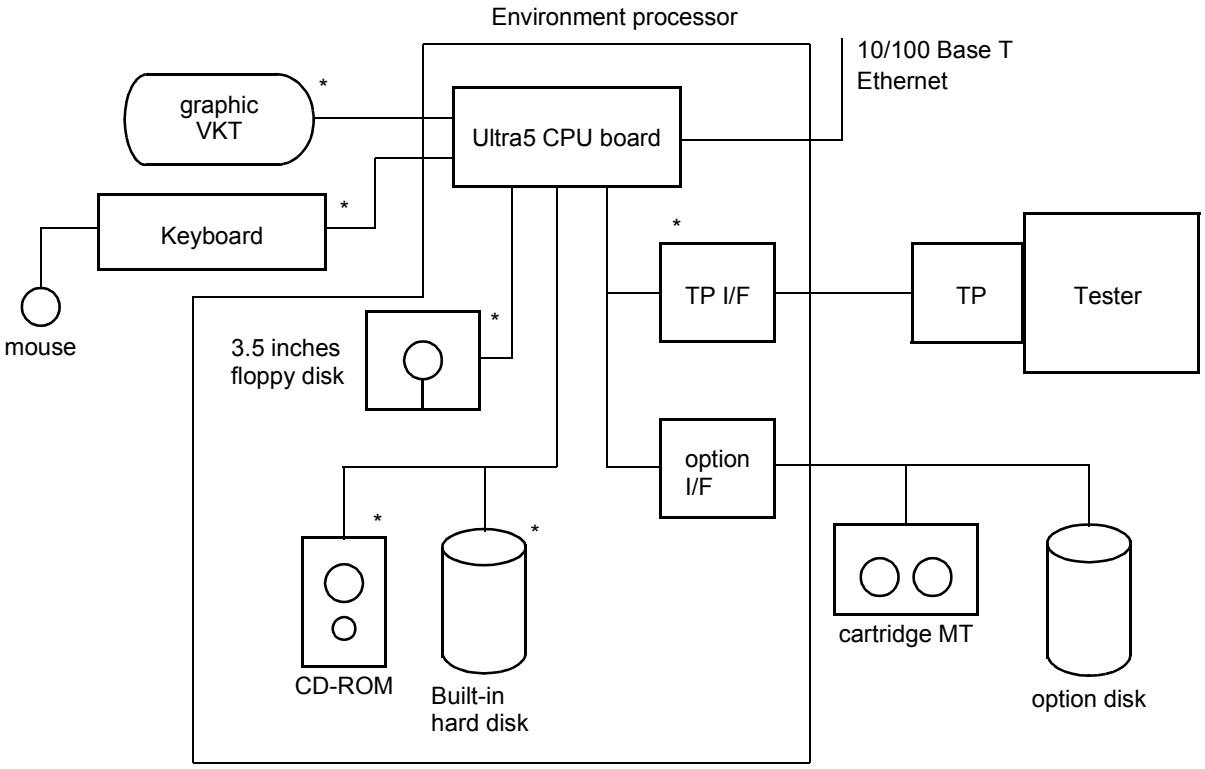
3.1.1 Environment Processor

The environment processor is the user's link to the tester. It controls all system functions, downloads test programs to the tester processor for execution and gathers the returned test results.

The workstation is the core of the environment processor. Although the current model uses the Ultra5 series of Sun Microsystems Inc., this model can replace it with the next generation high-performance workstation.

The functions of the environment processor include:

- User I/O
- File Management
- Edit and compile of programs
- Peripheral resource management
- Networking
- Test emulation
- Control of the test processor



Note: ***Each asterisk(*) indicates I/O peripherals provided as a standard.***

Figure 3-1 Computing System

3.1.2 Tester Processor

The tester processor executes the program that has been loaded into the test processor memory by the environment processor.

ADVANTEST has developed a special 32-bit tester processor for use in this memory test system. The tester processor is supervised by the environment processor to enhance the versatility and throughput of the test system.

The tester processor allows direct memory addressing in 32 M bytes and this addressing is also done to the tester registers and the tester memory. The tester processor allow transfer of data between memory blocks to be performed at a rate of 10 M bytes/sec by accessing each hardware resource with a single address space (that is, with a single instruction). Within the memory, tester control is handled as data; the maximum available rate of data transfer to the tester hardware can therefore be achieved.

Main features of the tester processor are listed below.

- 32-bit data word
- 24-bit address word
- Data transfer to all tester mainframe registers at 10 M bytes/sec

The major functions of the tester processor include:

- Interfacing between the environment processor and the tester hardware
- Compilation and execution of test programs

3.1.3 Peripheral Equipment

The standard configuration of the computing system includes the following peripheral equipments.

<Ultra5>

- Built-in hard disk(1 set)
- Color graphic monitor
- CD-ROM drive unit

The optional peripheral equipments are as follows:

- External hard disk
- cartridge MT unit

3.1.4 Station Control Boxes

Device test can be controled through the graphic terminal. Program editing, compiling, debugging and data processing can be made on the terminal at a time.

Each station has a control box, which provides control of program loading and execution. The control box is capable of enabling/disabling the data logging mode and the test abortion mode in the event of a test failure, and controlling all operational aspects of device tests.

The following control functions are provided:

- Loading of test program
- Selection of specific test number (for start, stop, or looping)
- Selection of debug modes such as loop of entire program and pause of test
- Selection of various data log options such as those for failures in functional tests or DC parametric measurements
- Abort or pause in the event of first failure
- Pause in the event of failure
- Selection of 16 function switches

The following can be displayed:

- DC parametric or function test results (PASS/FAIL)
- Device sort data
- Measured data
- Station status (READY, TESTING, TEST END, and ALARM included)

3.1.5 Communication with External Systems

This test system is available with two network interfaces to link the test system to external systems and to provide a friendly, integrated CAD/CAT network.

Ethernet Interface

ADVANTEST provides a network interface for Ethernet as a standard feature. It also provides the data link layer functions and part of the physical channel functions according to the ISO-OSI standard, as defined for Ethernet.

<SUN Ultra5>

This test system is equipped with the TCP/IP protocol software package as a standard. The object and source files generated by the host are down-loaded to this test system through the interface of the software package. On the other hand, the files that store the test plan developed at this test system, the test vector file, and the test results can be up-loaded to the host.

GPIB Interface

A GPIB interface is an available option and serves a dual function. The GPIB interface broadens system functionality by allowing an interface capability to external stimulus/measurement instruments.

4. SOFTWARE

4.1 General Description

This system operates under control of ASX/U-51 disk base system software (ADVANsite executive/ UNIX). The system software creates a test program, controls the test, performs automatic calibration, collects and analyzes test data, and controls system diagnostic routines.

4.2 System Software

Figure 4-1 shows the ASX/U-51 configuration that consists of the following three major software groups:

- Solaris (UNIX) software group (① to ④ of Figure 4-1)
- Offline software group (⑤ and ⑥ of Figure 4-1) for creation and editing of test programs
- Online software group (⑦ to ⑫ of Figure 4-1) consisting of the utilities that use tester resources and the tester controller and others that execute the test program.

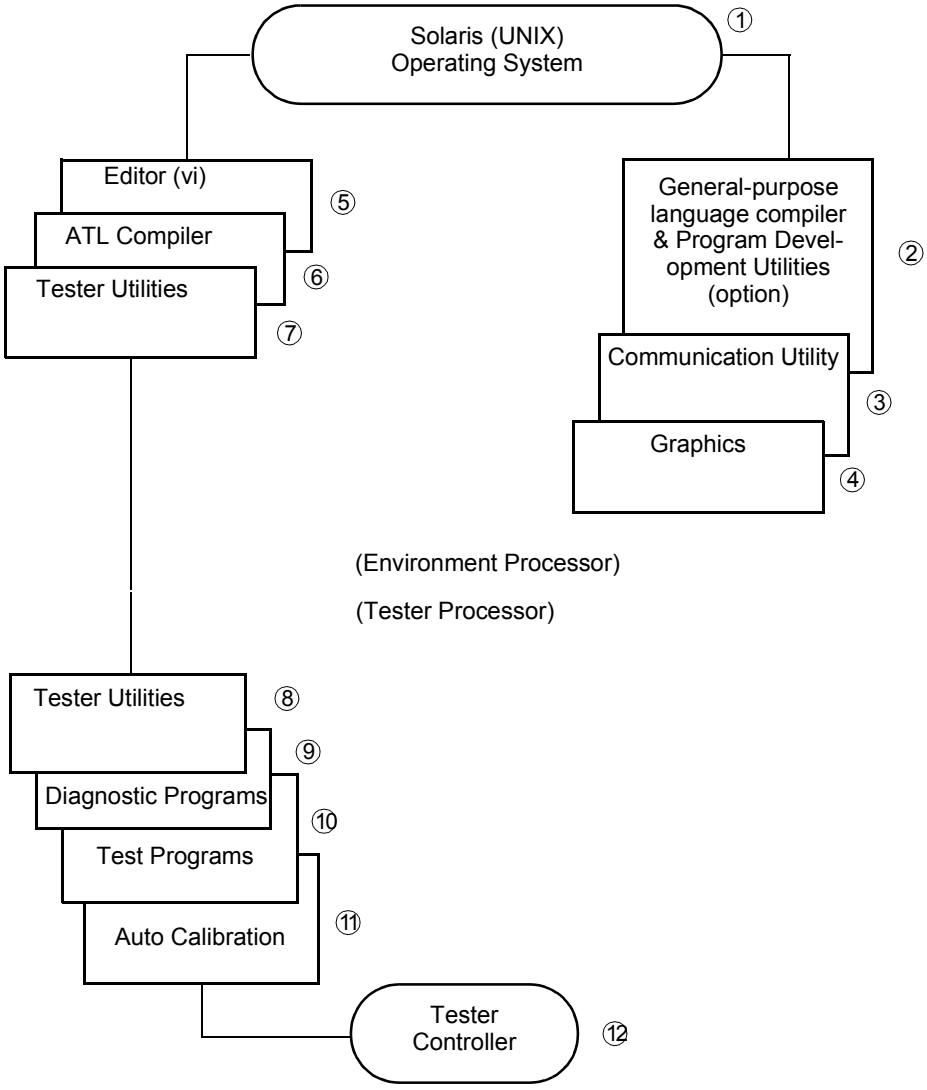


Figure 4-1 ASX/U-51 Structure

① Solaris (UNIX) Operating System

The Solaris (UNIX) operating system is a general-purpose virtual memory operating system used for time-sharing, batch processing, and real-time processing. This operating system contains commands for information interchange with the system, record management service, and run time libraries, in addition to the functions for process and time management, data structure support, memory management, input/output management, etc.

② General-purpose language compiler & Program Development Utilities (option)

- Sun WorkShop Professional C

③ Communication Utility

- Sun Link DNI (option)
- TCP/IP support

④ Graphics

- Open Windows

⑤ Editor

- Vi Editor
- Full-screen editor (Textedit)

⑥ ATL Compiler

The ATL-51 language compiler designed for the test program that runs on the tester processor. (option)

⑦ ⑧ Tester Utilities

Online utilities that mainly use the resources of the tester.
On the tester processor, each utility runs using the tester; on the environment processor, they provide user interfaces.
For details, see Section 4.6.

⑨ Diagnostic Programs

Self-diagnostic programs for the test system.

⑩ Test Program

The user program for MUT tests.
For details, see Section 4.3.

⑪ Auto-calibration

The program for automatic calibration of timing, voltage, and current accuracies.

⑫ Tester Controller

Programs that consist of the supervisor, tester driver, etc. for the tester processor.

4.3 Test Programs

There are two major types of device test programs: the test execution programs and the memory pattern (MPAT) programs (see Figure 4-2). Each program has the compiler to compile the source program into the object program. All programs including test programs and utilities are managed as files even if they are in the source format or object format.

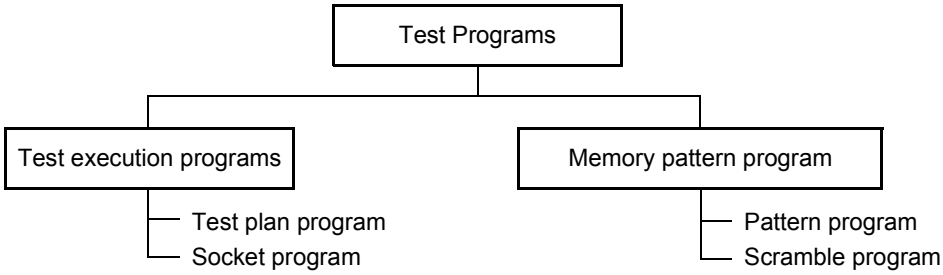


Figure 4-2 Test Program Configuration

4.3.1 Test Plan Program

The test plan program sets the test conditions, specifies the execution statements for DC parametric test and functional test, and controls the entire test sequence.

The test plan programs can be written as a single device measuring program even when two or more devices are measured simultaneously.

4.3.2 Socket Program

The socket program defines the relationship between pin names used for test plan program and pin numbers of the test system. If this socket program is used, the DUT pin numbers can be specified in the test plan program without using pin numbers of the test system.

If multiple devices are measured simultaneously and if its information is defined in the socket program, the test plan program can function as the multi-socket program. The test plan programs are commonly used for a single socket and for multiple sockets. The handler control and prober control are supported automatically.

4.3.3 Pattern (MPAT) Program

The pattern (MPAT) program defines the test vector according to the MUT test data. This MPAT program is selected by the test plan program and executed.

4.3.4 Scramble (SCRAM) Program

The scramble (SCRAM) program defines the replacement expression for correction of MUT decode topology and address topology. The X, Y and Z address vectors are replaced and output according to these data.

4.4 Test Language

This system uses the Advantest test language (ATL) for test programming. The ATL has been developed by Advantest Corp. and it features the easy-to-learn and easy-to-use expansion type FORTRAN language. The program can be modified or debugged quickly.

The ATL provides the constant, calculation expressions, and measuring condition setup functions. It can handle up to three-dimensional arrays, and it provides various jump, branch and loop functions. This is helpful to create a structured program having easy-to-read structure.

4.5 Test Plan

Figure 4-3 shows a test plan flow from program creation and compiling to program loading and execution.

When the program is compiled, a file name is added to it and stored on the disk. When the program file name is specified from the operator console and when the Start switch is pressed on the console, the program is executed. When specified by the program, the tester driver controls the test station requested for startup and executes the program.

As the user can modify the test conditions and log the new test results by using the utility program, he or she needs not recompile the source program.

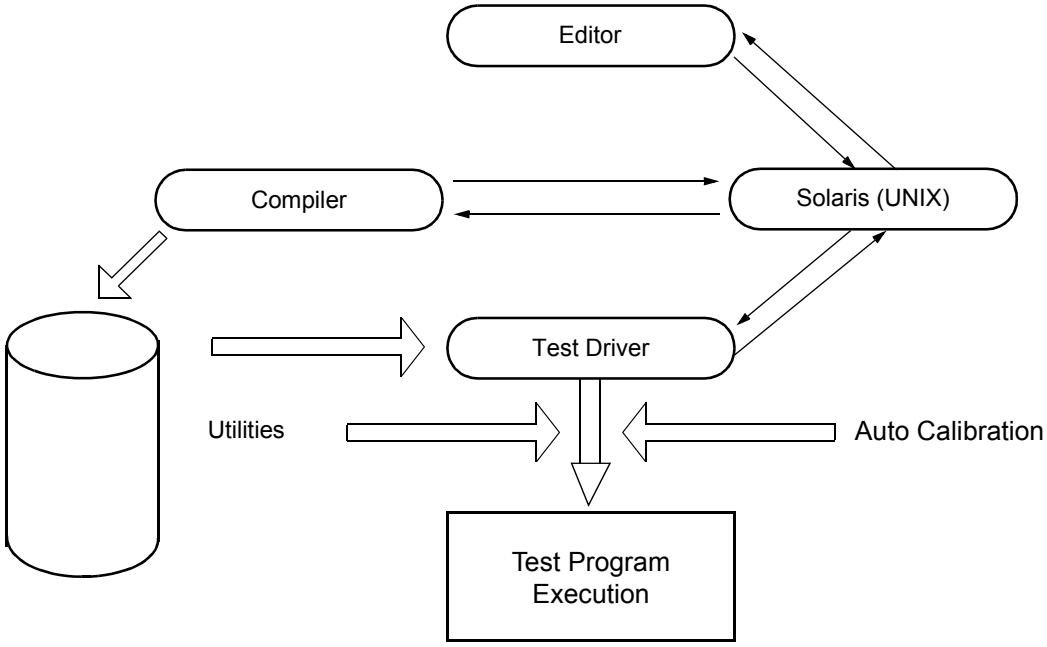


Figure 4-3 Test Plan

4.6 Tester Utility

ASX/U-51 provides a wide variety of utilities which reduce program debugging time and improve the flexibility and throughput of device engineering.

These utilities can be used by specifying a specific MUT, regardless of whether multi-socket or single-socket is used, and therefore are useful for debugging multi-socket programs and analyzing devices.

The utilities provided for ASX/U-51 are listed below. All utilities are stored on disk, and each is called through an operator console.

4.6.1 Pin Monitor

This utility displays each test condition (pin connection, V_{IL}/V_{IH}, V_{OL}/V_{OH}, timing edge, DC parametric test, device power supply, etc.) that is programmed, at the point in the program at which it is invoked.

4.6.2 Data Set

This utility modifies various values that have been set (driver and comparator voltages, timing edge, DUT power supply, etc.) at the points in the test program at which they are invoked.

4.6.3 Data Scan

If the same test is repeated using one parameter (such as VCC), this utility automatically varies the parameter to observe the effect (“software joystick”).

4.6.4 Debugger

This utility sets break points at any desired points in an object program, and temporarily halts the testing at these break points. This enables the insertion of condition setting statements into the object code without the overhead of editing and compiling.

4.6.5 2D/3D SHMOO Plot

This utility sets an arbitrary parameter on the X/Y axes at any point during the execution of a test program, to display a pass/fail plot. A three-dimensional SHMOO plot can be obtained easily and quickly by setting the Z axis as well. Any tester parameter can be “tracked” by any other parameters, so that each voltage or timing condition can be controlled during a SHMOO plotting sequence.

4.6.6 Wafer Map

During the execution of a wafer probe test, the results of the test (DC, FUNC test and bin sorting) are displayed as a wafer map.

4.6.7 Histogram Creation Program

This collects the results of DC parametric tests, and outputs histograms, average values, maximum values, minimum values and standard deviations.

4.6.8 MPAT Tracer

This displays the status of the ALPG operation, specifically the X, Y, and Z address data and read/write response data based on the vector generation sequence.

4.6.9 Datalog

Datalogging can be performed by specifying numerous modes from an operator console.

5. SPECIFICATION FOR INSTALLATION AND ACCEPTANCE

This test system can use two types of chiller shown below.

The installation procedure differs depending on the chiller type. Check the chiller type and install the test system correctly.

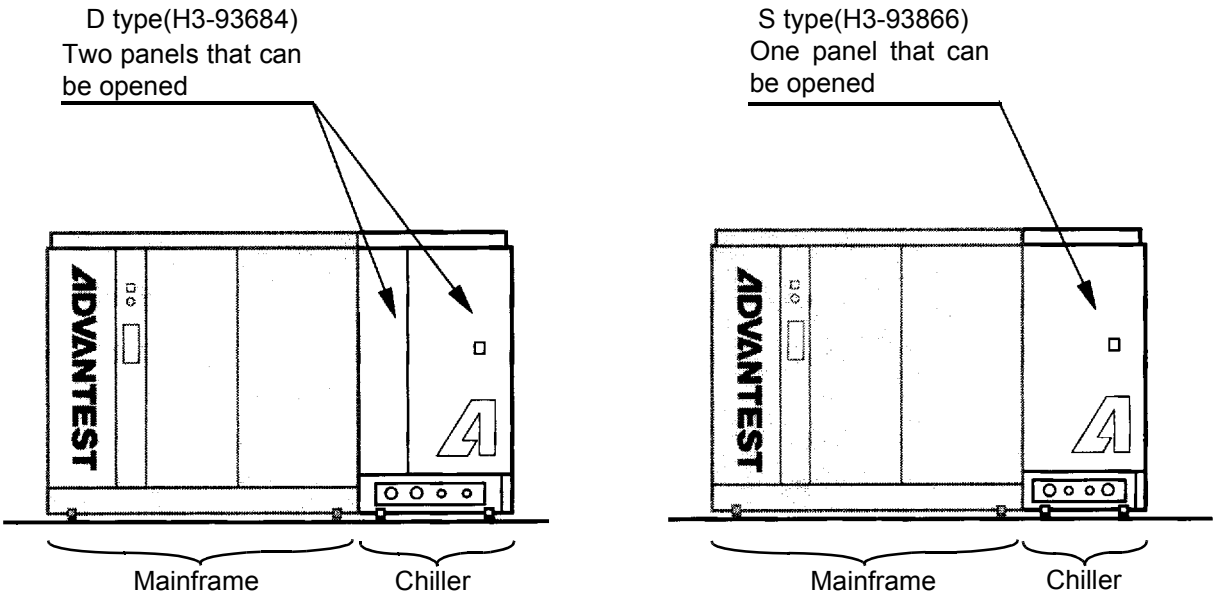


Figure 5-1 Chiller Types

5.1 Installation Plan

5.1.1 Environmental Requirements

This system must be installed in a place with the following ambient conditions:

- Temperature
  In operation : 25°C ± 5°C
  When stopped : -20°C to +50°C
  (-20°C to +40°C for Sun machine and its peripherals)
  Changes of temperature must be less than 2°C/hour.
- Relative humidity
  In operation : 20% to 65%
  When stopped : 20% to 90%

Shock must be less than 3 G when the system is being moved. When this system is installed on site, vibration must not exceed 0.2 G at 5 Hz to 50 Hz, or 0.5 G at 50 Hz to 500 Hz.

Dust in the air at the installation site must be less than 0.1 mg/m^3. Environments with high levels of salinity, iron, or corrosive gases are not recommended.

5.1.2 Power Requirements

The number of power lines for the test system differs depending on the chiller type.

For the D type chiller: Six power lines of 200 VAC and three phases

For the S type chiller: Five power lines of 200 VAC and three phases

- Common Mode surges should not exceed 1000 V for the AC power supply input. If it is possible that Common Mode surges exceeding 1000 V will occur, appropriate countermeasures must be taken.
- Differential Mode surges should not exceed 500 V for the AC power supply input. If it is possible that Differential Mode surges exceeding 500 V will occur, appropriate countermeasures must be taken.
- Surges should not exceed 250 V for external interface cables. If it is possible that surges exceeding 250 V will occur, appropriate countermeasures must be taken.
- Voltage interruptions must be not longer than 10 ms.
- Electrical fast transient/burst voltage must be less than 2000 V for AC power supply or according countermeasures must be taken.

Electrical fast tansient/burst voltage must be less than 1000 V for external interface cables or according countermeasures must be taken.

Voltage and frequency stability requirements are as follows:

180 VAC to 220 VAC three-phase 50/60 Hz $\pm$ 0.5%

If voltage fluctuations are outside this range, a regulator must be used.

Each power supply must be connected via the 30-mA circuit breaker having the grounded terminal.

The ground resistance for the ground connection must be 100 Ω or less. Prepare the power cable (_____ lines in Figure 5-2) and use the following crimp contacts for connection to the tester.

Crimp Terminal:	Outside diameter	15 mm
	Screw hole diameter	6.4 mm

(The power cable includes a wire, which is used to connect the test system and the frame ground. However, this wire is unused.)

To connect the separated frame ground wire between the power switchboard and test system, use the crimp terminal and wire specified below.

Wire size:	AWG 1, Green and yellow spiral pattern (UL1284 compatible)	
Crimp Terminal:	Outside diameter	15.5 mm
	Screw hole diameter	5.3 mm

Connect pins for the power input terminals of the tester side in order of R $\rightarrow$ S $\rightarrow$ T (U $\rightarrow$ V$\rightarrow$ W) from the left side of the operation panel to prevent from inverse rotation of three-phase AC fan. (Confirm that wind blows from the whole surface of the upper side of the cabinet when the power turns on.)

Power requirements are given in Table 5-1.

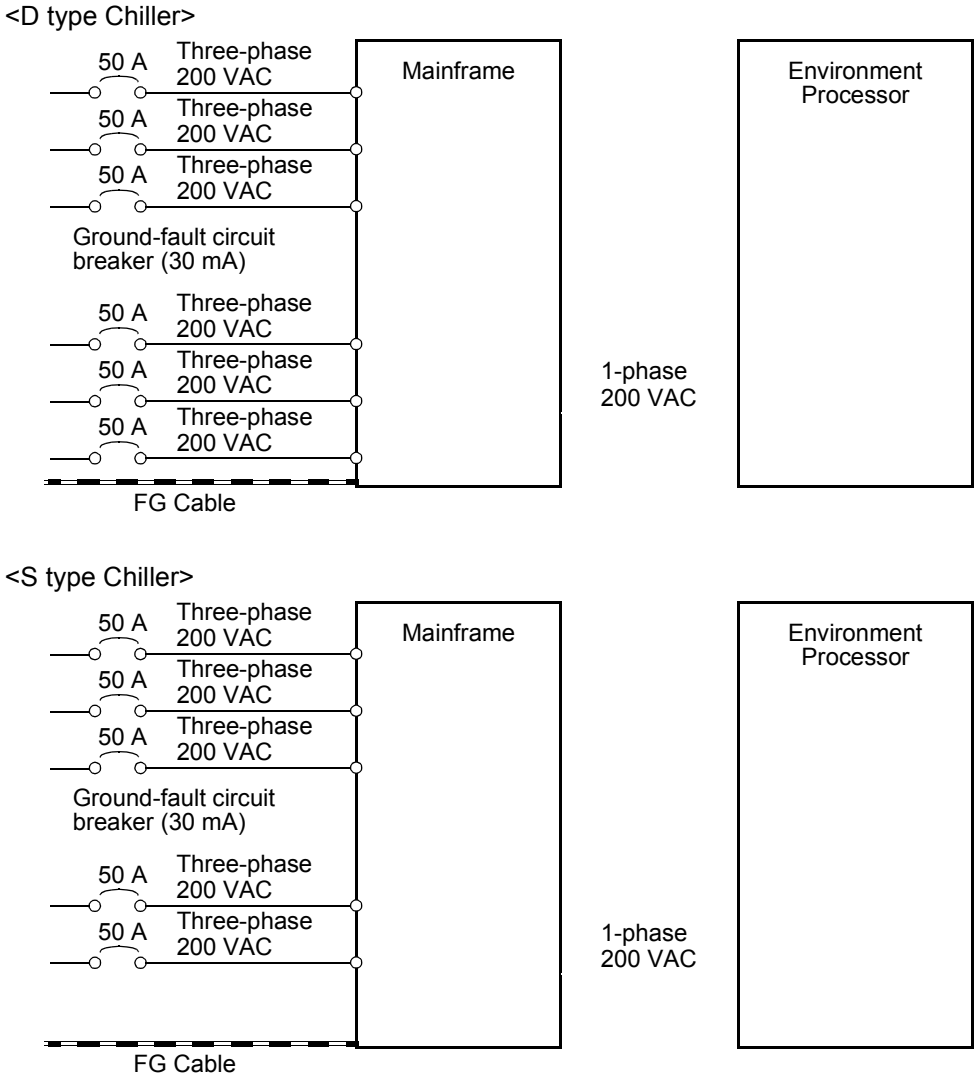


Figure 5-2 Power Supplies

Table 5-1 Power Consumption

System	Maximum configuration for 2STN	Maximum configuration for 1STN
D type Chiller	68 kVA	46 kVA
S type Chiller	60 kVA	37 kVA

Main Circuit Breaker interrupting capacity: 10 kA
(30 kA: When the undervoltage release control is attached.)

5.1.3 Air Conditioning Requirements

The T5592 is supplied with cooling water, which absorbs almost all of the heat generated by the mainframe and test head.

The heat generated by this system is given in Table 5-2. These values must be taken into consideration for air conditioning requirements. An air conditioner must be provided for the room where the test system is installed.

Table 5-2 Amount of Heat Generated

Maximum configuration for 2STN	Maximum configuration for 1STN
4200KJ	2400KJ

5.1.4 Compressed Air

(1) This system requires the following air source for mounting/dismounting the performance board.

- Air source : 0.49 to 0.69 MPa (dry air)
- Air consumption : 5 to 10 Nℓ /min

(2) Air supply hose and hose clamp must be prepared by the customer.

Air hose connector will be delivered by ADVANTEST.

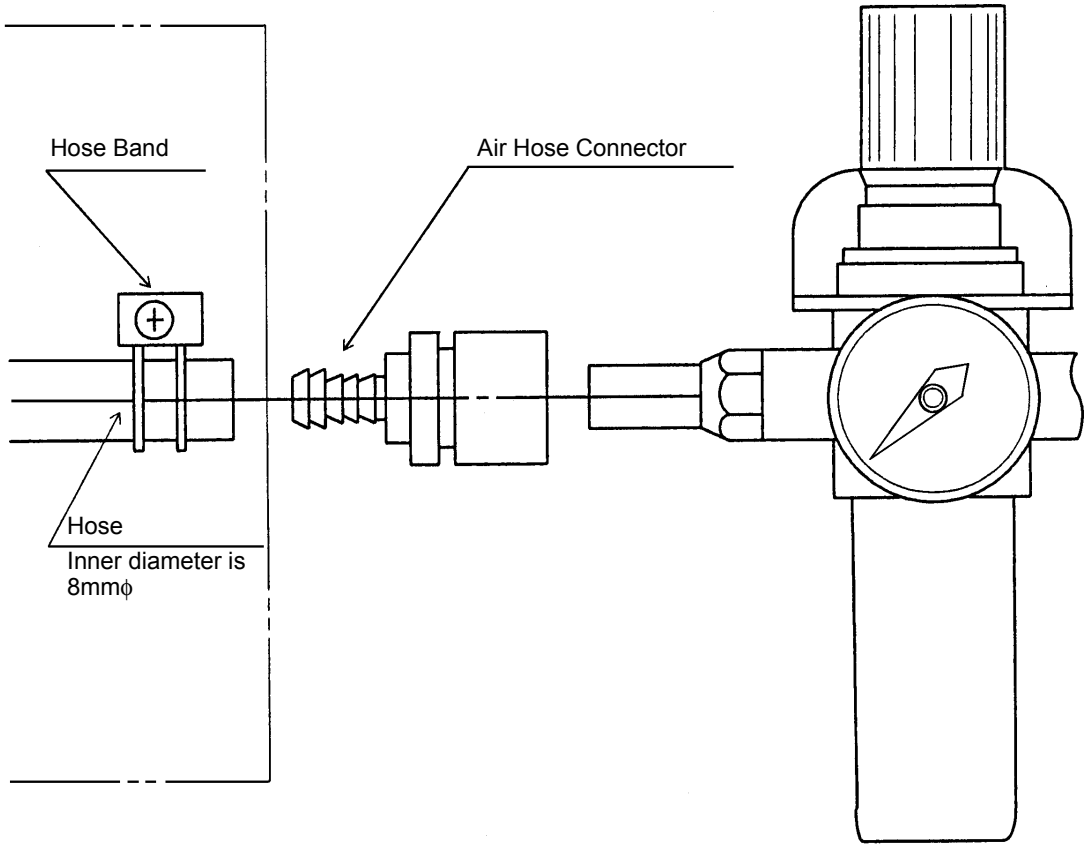


Figure 5-3 Connection

5.1.5 Floor Plan

Floor plans of standard system configurations are shown in Figure 5-4 to Figure 5-11.

The mainframe should be installed with its rear surface approximately 1 meter away from the wall, to provide a maintenance work area.

The height of the room from floor to ceiling must be at least 2600 mm for system maintenance.

The outer dimensions (height x width x depth) for the mainframe are shown below.

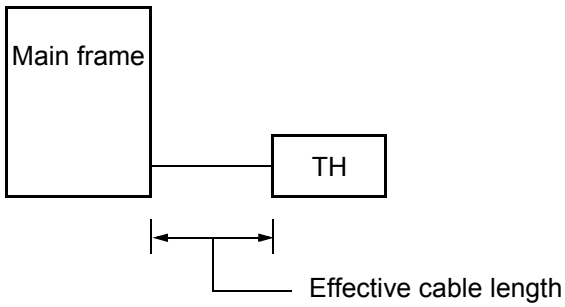
- For the D type chiller test system: 1900 mm x 3050 mm x 950 mm
- For the S type chiller test system: 1900 mm x 2850 mm x 950 mm

Movable distance of each section is also shown in Table 5-3.

Table 5-3 Movable Distance

Each Portion Names	Starting Points	Effective cable length
Test Head	Front side of mainframe	4 m approx. (Note 1)
EWS	Rear side of mainframe	8 m approx.
Graphic Monitor	Rear side of EWS	1 m approx.

Note1: "Effective cable length" in the table refers to that shown below.



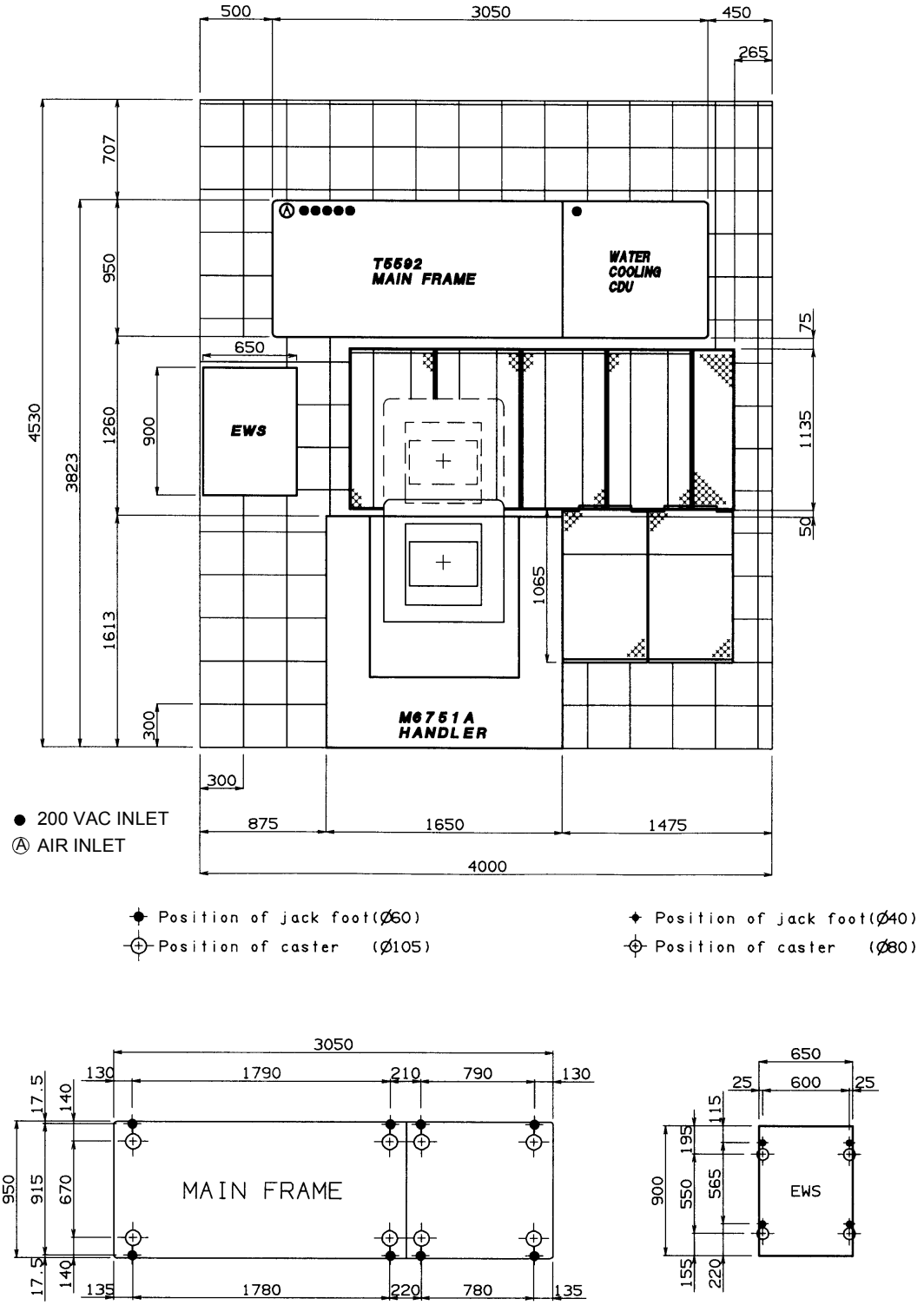


Figure 5-4 T5592(D Type Chiller)+M6751A System Layout (1STN)

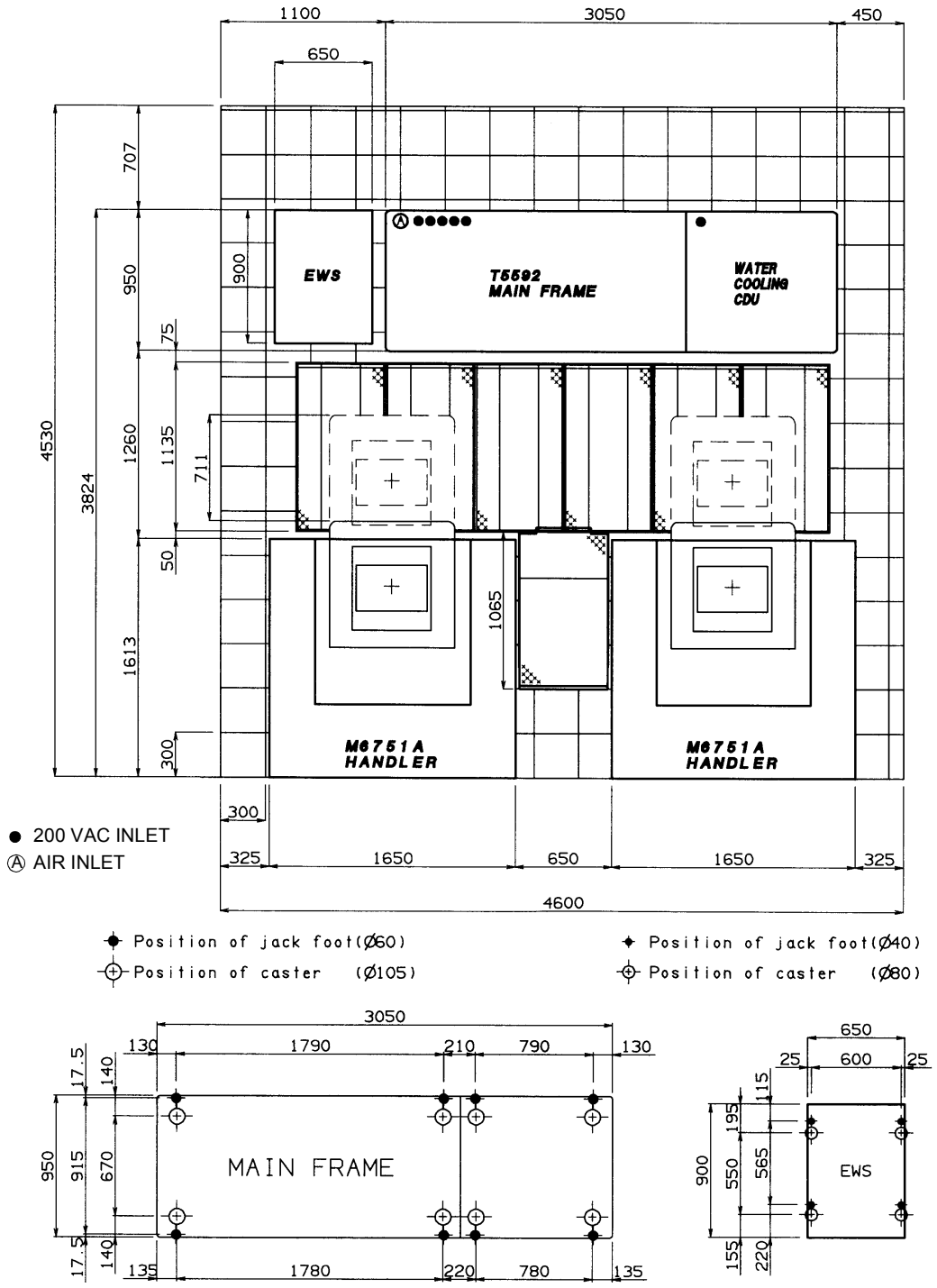


Figure 5-5 T5592(D Type Chiller)+M6751A System Layout (2STN)

Three cable ducts are installed between the two handlers.

Make sure that there is at least 650 mm of space between the two handlers in order to have enough room to install additional hardware as required.

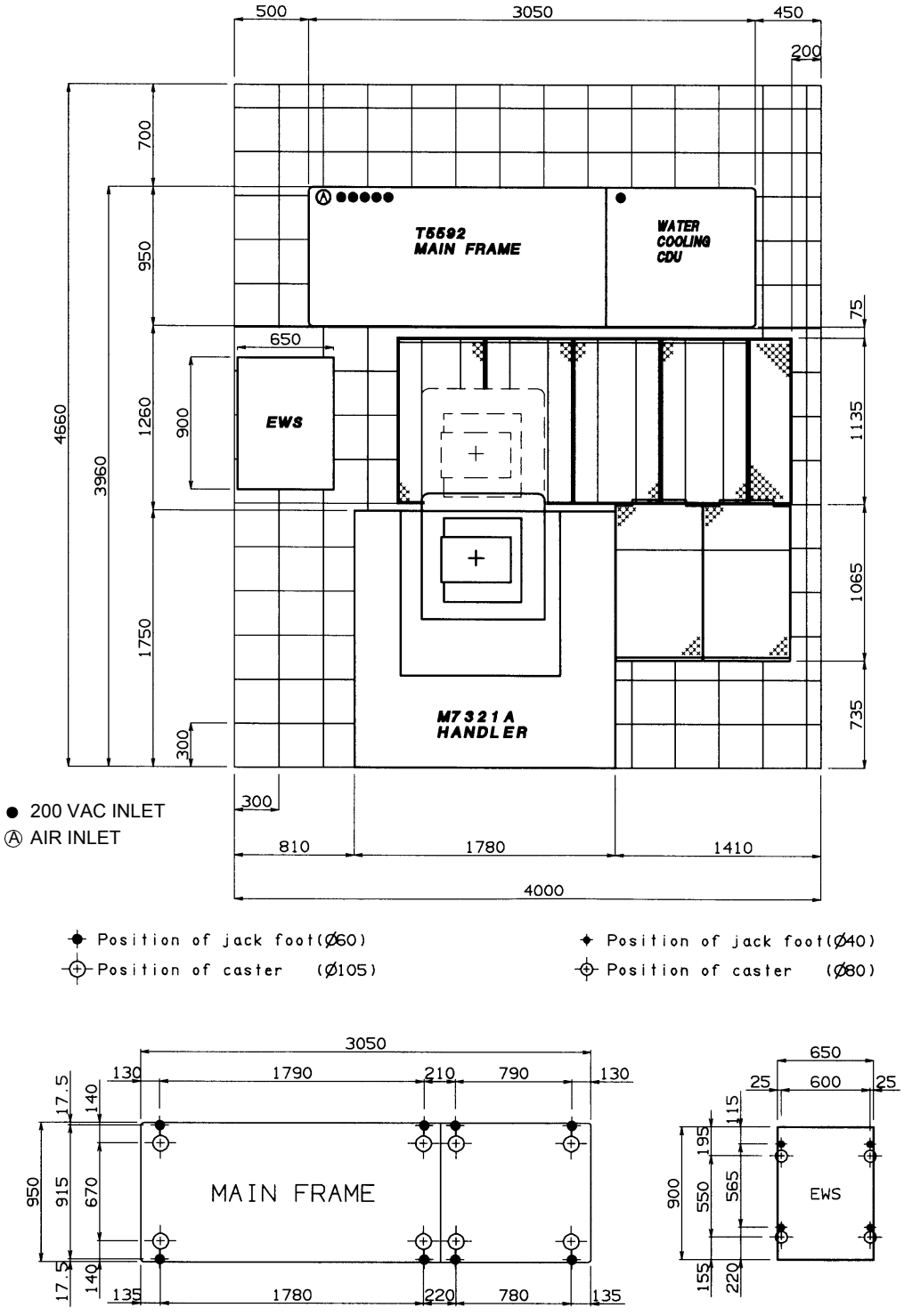


Figure 5-6 T5592(D Type Chiller)+M7321A System Layout (1STN)

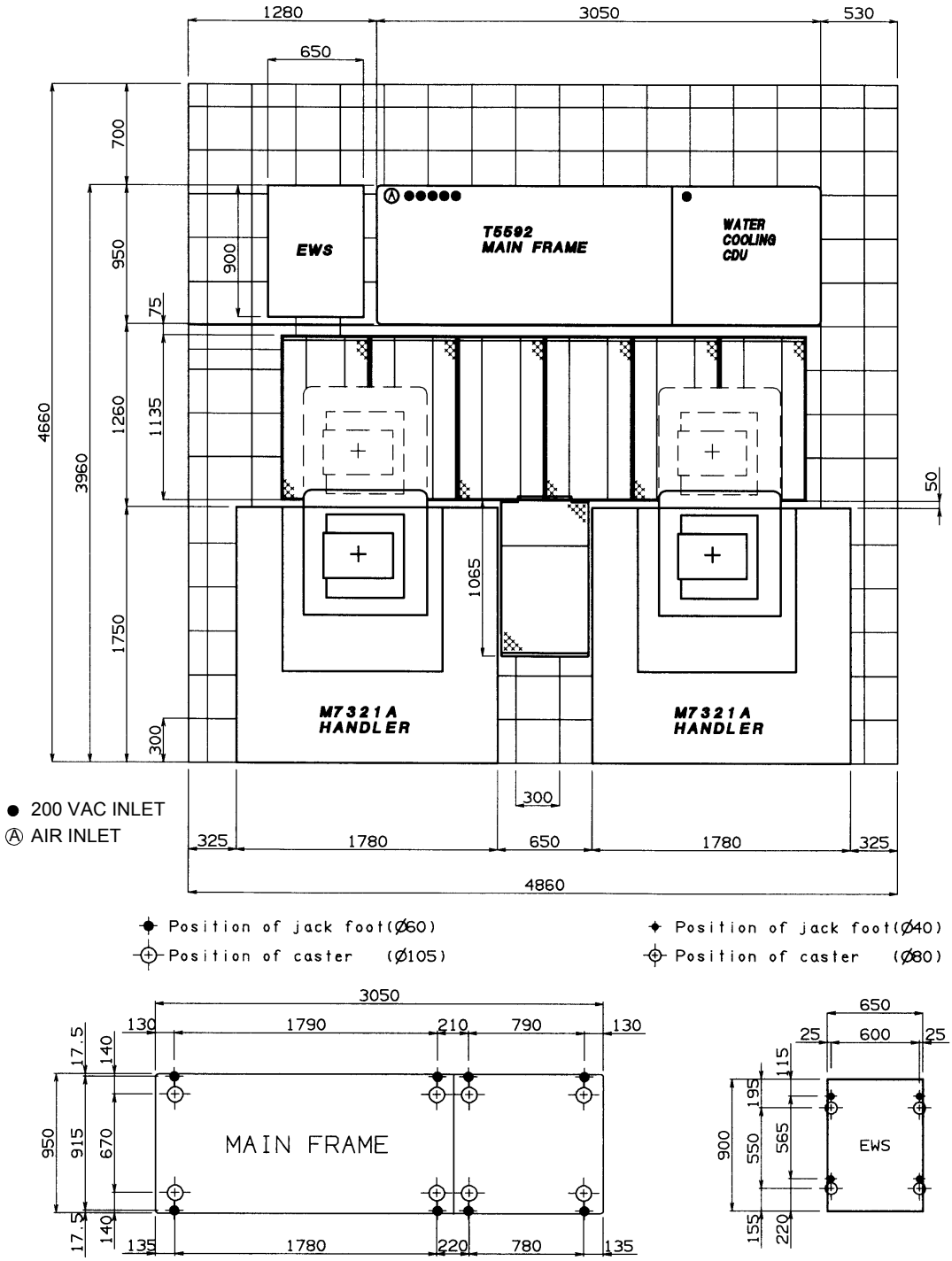


Figure 5-7 T5592(D Type Chiller)+M7321A System Layout (2STN)

Three cable ducts are installed between the two handlers.

Make sure that there is at least 650 mm of space between the two handlers in order to have enough room to install additional hardware as required.

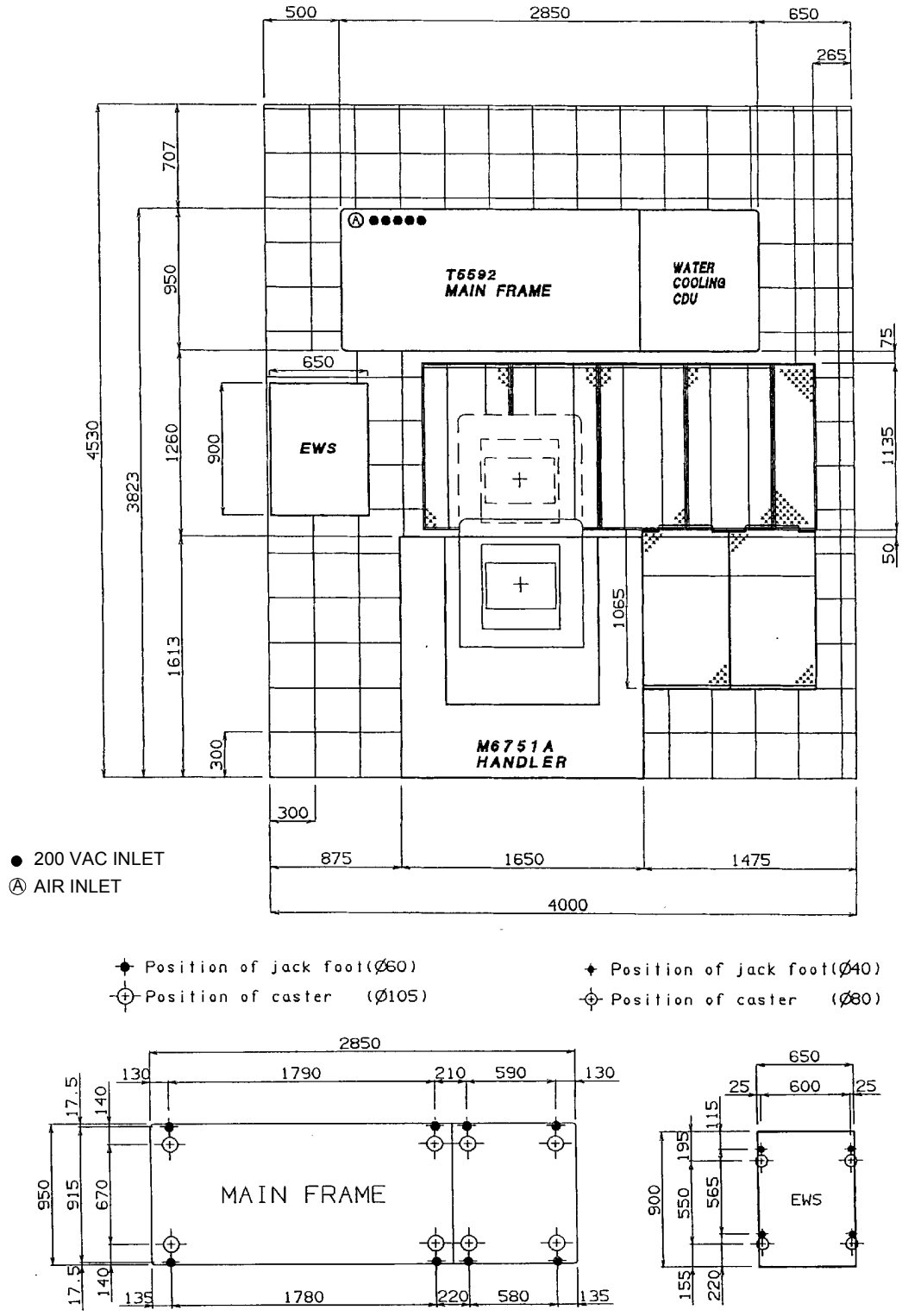


Figure 5-8 T5592(S Type Chiller)+M6751A System Layout (1STN)

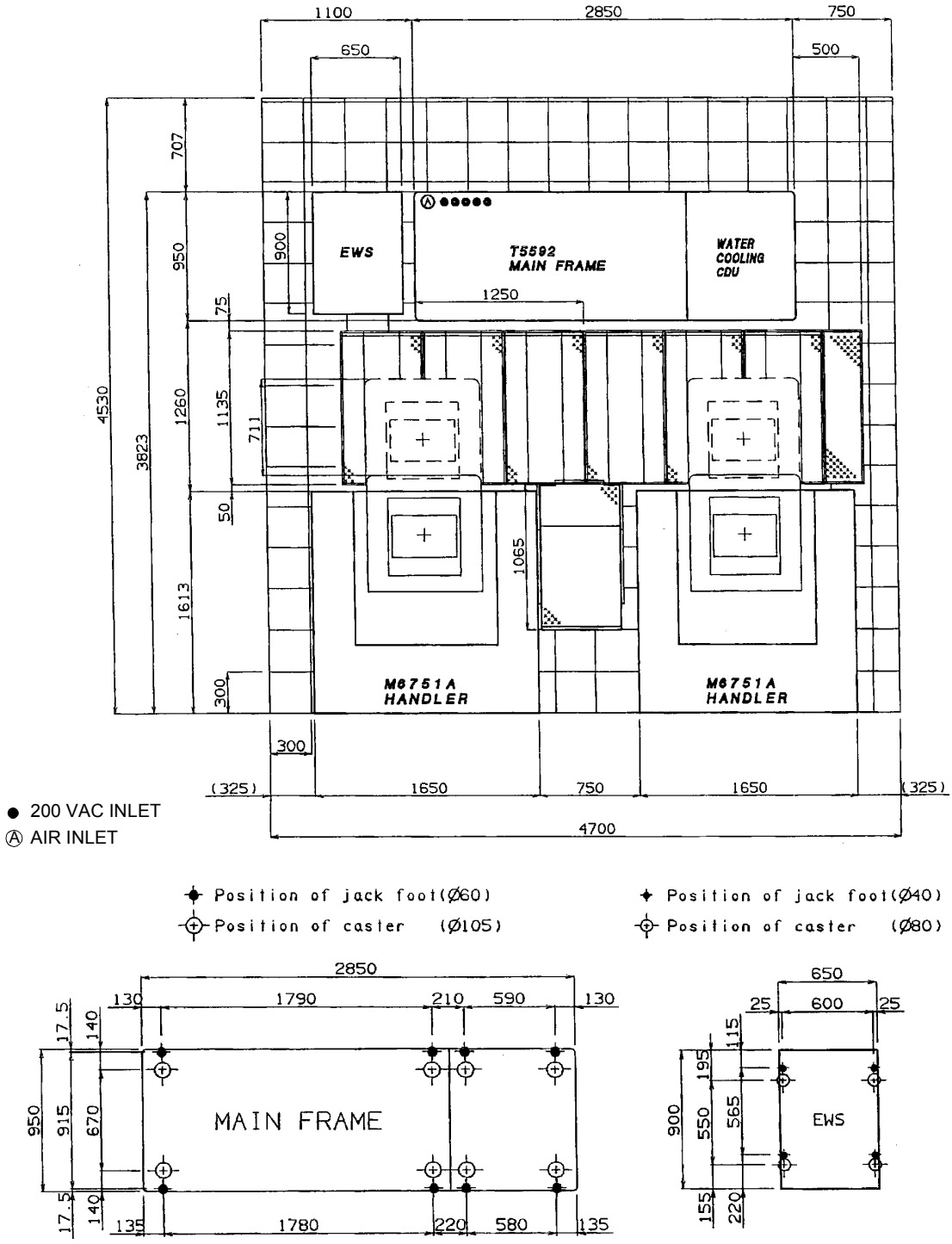


Figure 5-9 T5592(S Type Chiller)+M6751A System Layout (2STN)

Three cable ducts are installed between the two handlers.

Make sure that there is at least 650 mm of space between the two handlers in order to have enough room to install additional hardware as required.

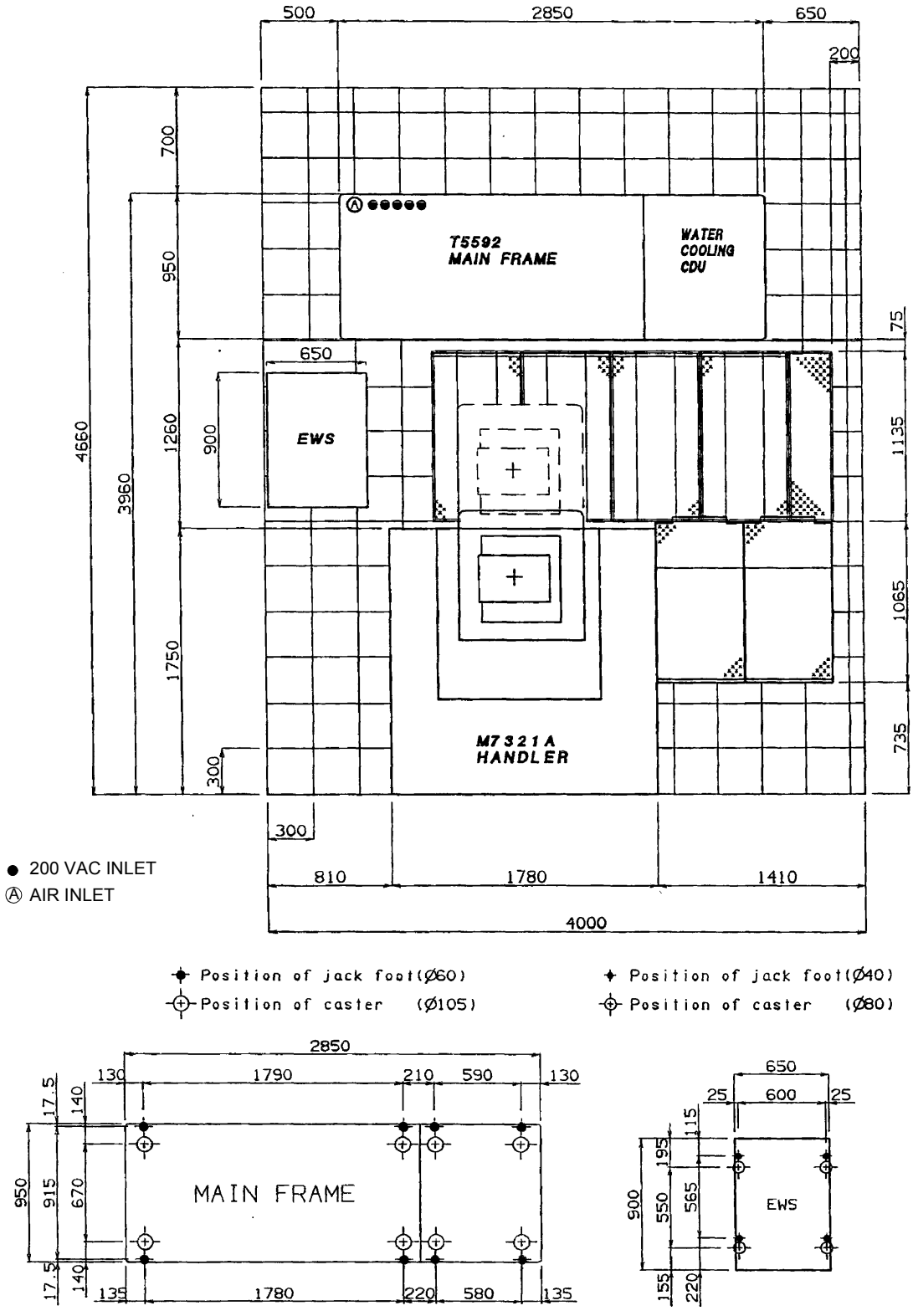


Figure 5-10 T5592(S type Chiller)+M7321A System Layout (1STN)

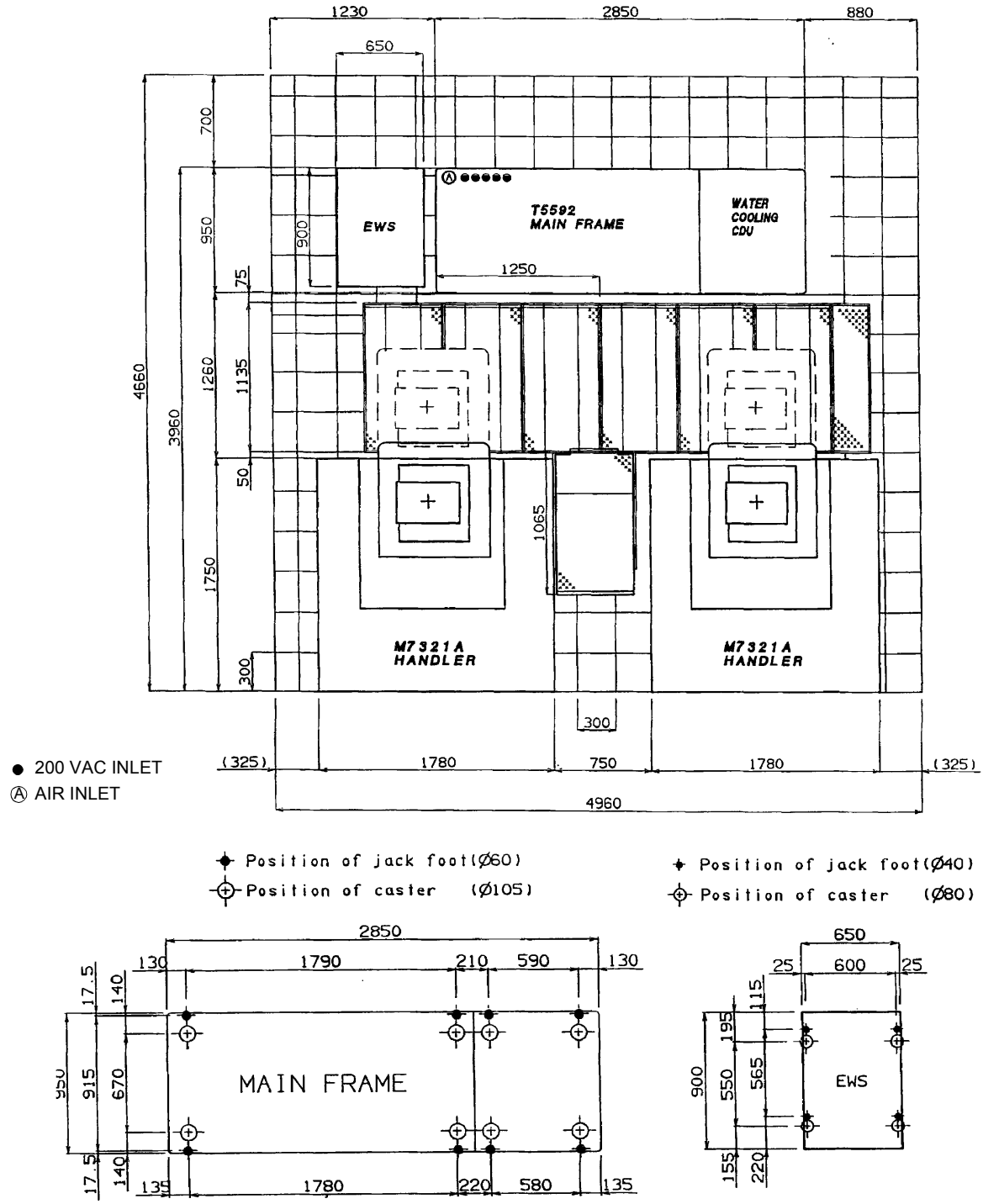


Figure 5-11 T5592(S Type Chiller)+M7321A System Layout (2STN)

Three cable ducts are installed between the two handlers.

Make sure that there is at least 650 mm of space between the two handlers in order to have enough room to install additional hardware as required.

5.1.6 System Mass

Table 5-4 System Mas

	D Type Chiller	S Type Chiller
Mainframe	1900 kg	1780 kg
Test head	350 kg	
EWS (including a 21-inch monitor)	45 kg	
1/4" cartridge MTU	4 kg	
2.1G-byte disk drive	5 kg	
System desk	20 kg	

5.1.7 Tester Name Plate

When operating several systems, it is convenient to put a name on each component of the system.

Alphanumerics can be written on the name plate on the left-hand side of this system mainframe which has been provided on customer request.

A maximum of five alphanumerics can be written after the T5592 designation.

Example: T5592 AT1

5.1.8 Carriage Requirements

- Floor strength: 4.9 kPa to 9.8 kPa
- Building entrance: (Wide) 2 meters or more
  (Height) 3 meters or more
- Carriage path: (Wide) 1.8 meters or more
  (Height) 2.5 meters or more
- Laboratory entrance: (Wide) 1.5 meters or more
  (Height) 2.5 meters or more

5.1.9 Earthquake-proof

ADVANTEST provides fixtures to protect test systems and their peripheral devices against earthquake damage.

The fixtures must be secured to the floor with anchor bolts. Thus, the location of the test systems must be determined in advance.

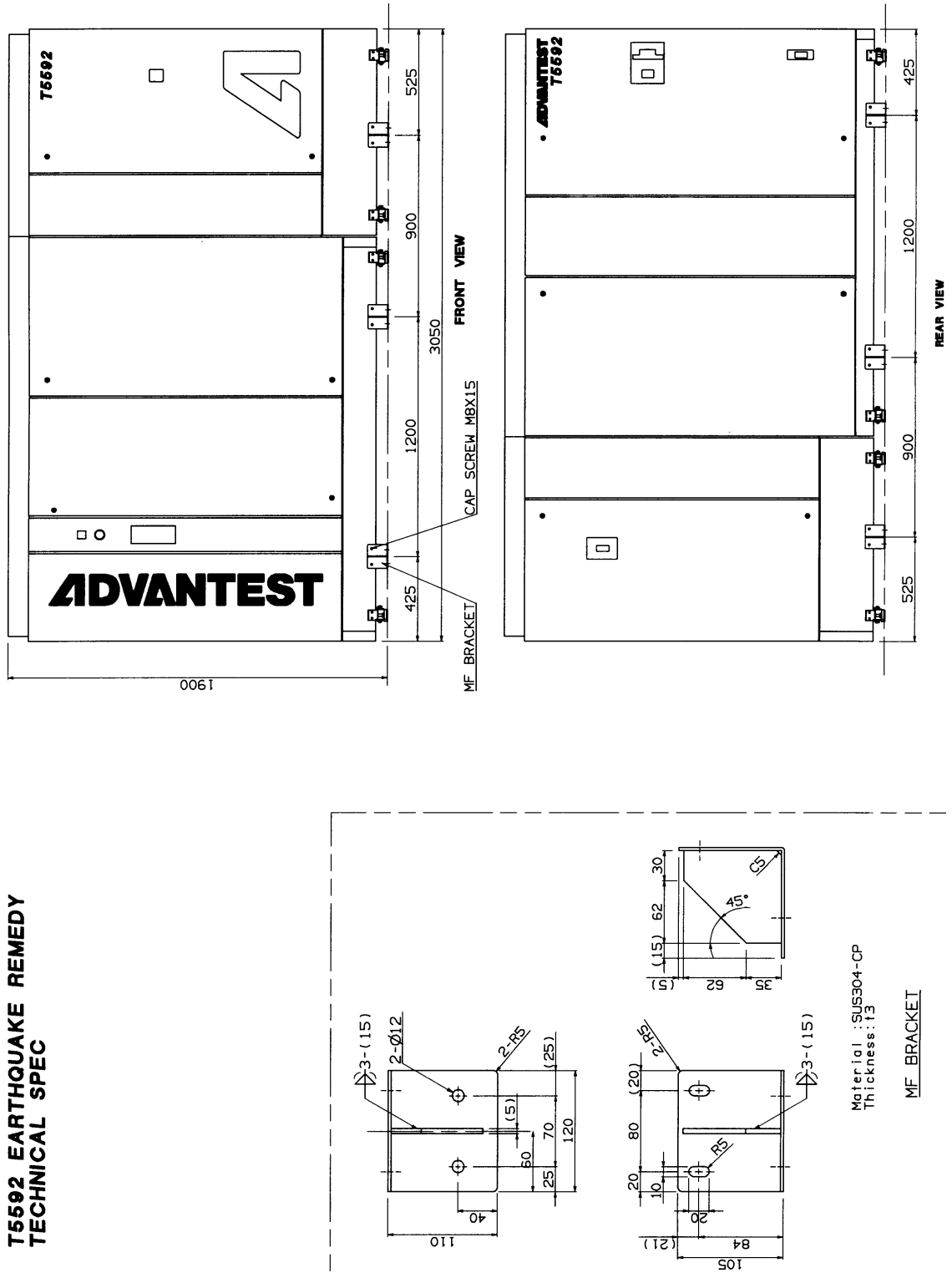


Figure 5-12 T5592 Earthquake Remedy Technical Spec(D Type Chiller)

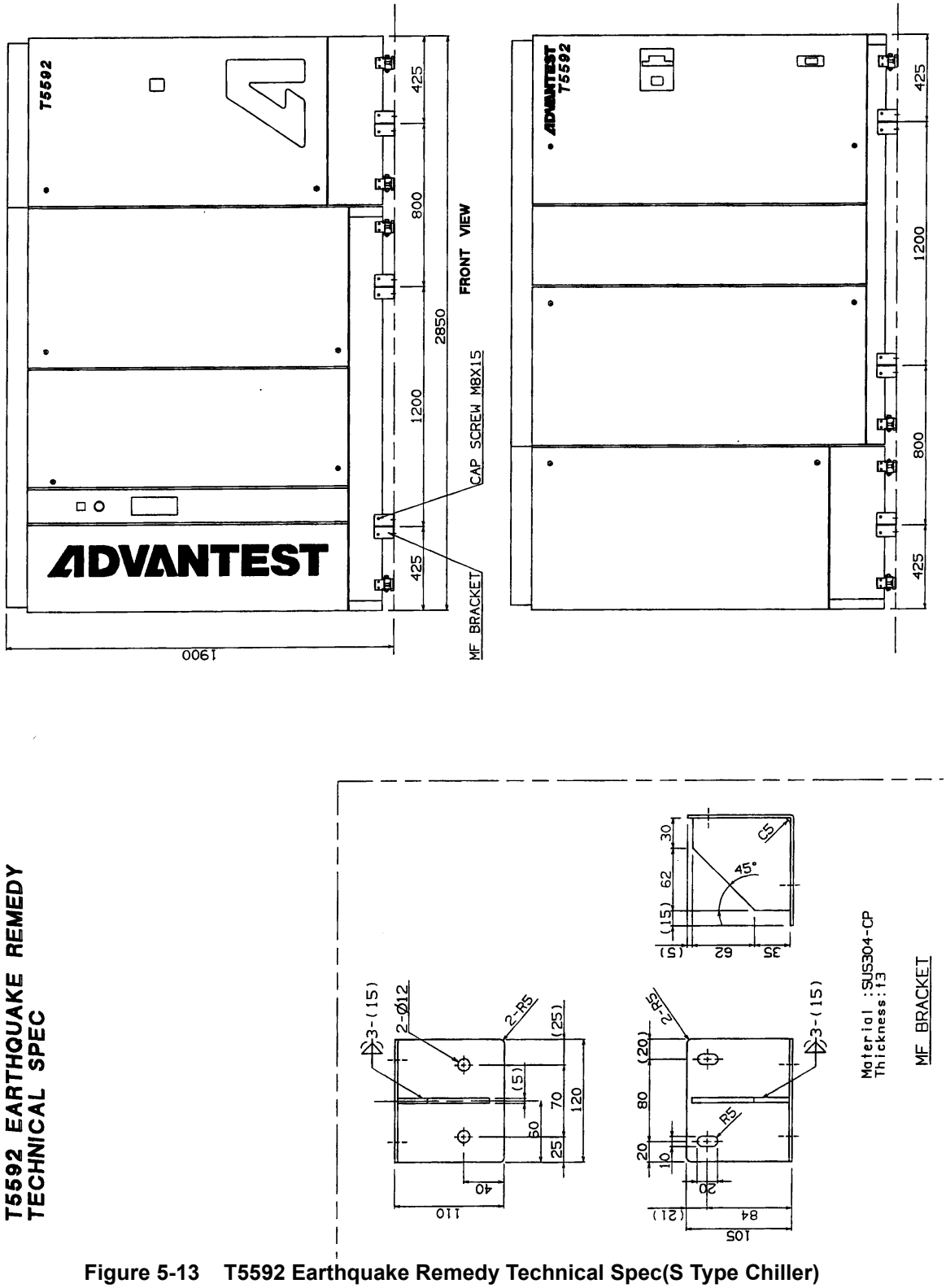


Figure 5-13 T5592 Earthquake Remedy Technical Spec(S Type Chiller)

5.1.10 Cooling Water

(1) Cooling Water Supply Conditions

<D type chiller>

The cooling water must satisfy the following conditions:

Temperature range:	7 °C through 20 °C
Temperature variation:	1 °C or less per 10 min.
Flow rate:	80 L/min. through 250 L/min.
Flow rate variation:	5 %/min. or less
Pressure:	0.2 MPa through 0.7 MPa

The flow rate and pressure loss vary depending on the cooling water temperature as shown in the table below.

Table 5-5 Flow Rate and Pressure Loss

Cooling water temperature	Flow rate	Pressure Loss
7 °C	80 L/min.	0.04 MPa
12 °C	110 L/min.	0.10 MPa
16 °C	160 L/min.	0.21 MPa
20 °C	250 L/min.	0.37 MPa

<S type chiller>

The cooling water must satisfy the following conditions:

Temperature:	7 °C through 20 °C
Temperature variation:	1 °C or less per 10 min.
Flow rate:	27 L/min. through 90 L/min.
Flow variation:	5 %/min. or less
Pressure:	0.2 MPa through 0.7 MPa
Return Pressure:	0.3 MPa or less (The return pressure must be at least 0.2 MPa lower than the pressure used to supply the cooling water.)

The flow rate varies depending on the cooling water temperature as shown in the table below.

Table 5-6 Flow Rate

Cooling water temperature	Flow rate
7 °C	28 L/min.
12 °C	33 L/min.
16 °C	45 L/min.
20 °C	90 L/min.

(2) Water Quality

The cooling water must meet the following conditions:

Standard Materials

pH (25°C)			:	6.8 to 8.0
Conductivity (25°C)		(μS/cm)	:	400 or less
Chloride ion	Cl^-	($mgCl^-/l$)	:	50 or less
Sulfate ion	SO_4^{2-}	($mgSO_4^{2-}/l$)	:	50 or less
Acid consumption (pH 4.8)		($mgCaCO_3/l$)	:	50 or less
Total hardness		($mgCaCo_3/l$)	:	70 or less

Reference Materials

Iron	Fe	(mgFe/l)	:	1.0 or less
Sulfide ion	S^{2-}	(mgS^{2-}/l)	:	No detection
Ammonium ion	NH_4^+	($mgNH_4^+/l$)	:	1.0 or less
Ionized silica	SiO_2	($mgSiO_2/l$)	:	30 or less

The above items are taken from the water quality standard (JRA-GL-02-1994) of the Japan Refrigeration and Air Conditioning Industry Association.

The chiller plumbing is not intended to use pure water.

5.1.11 Plumbing Specifications

<D type chiller>

(1) Plumbing conditions

The plumbing positions and sizes used for the D type chiller are listed below.

① Cooling water inlet (with a valve) Two positions
Female taper pipe thread: Rc1 1/4 (ISO 7/1 PT 1 1/4 compliant)

② Cooling water outlet (with a valve) Two positions
Female taper pipe thread: Rc1 1/4 (ISO 7/1 PT 1 1/4 compliant)

③ Drain for the chiller (with a plug) One position
Female taper pipe thread: Rc 1/2 (ISO 7/1 PT 1/2 compliant)

④ Drain for the mainframe (with a plug) One position
Female taper pipe thread: Rc 1/2 (ISO 7/1 PT 1/2 compliant)

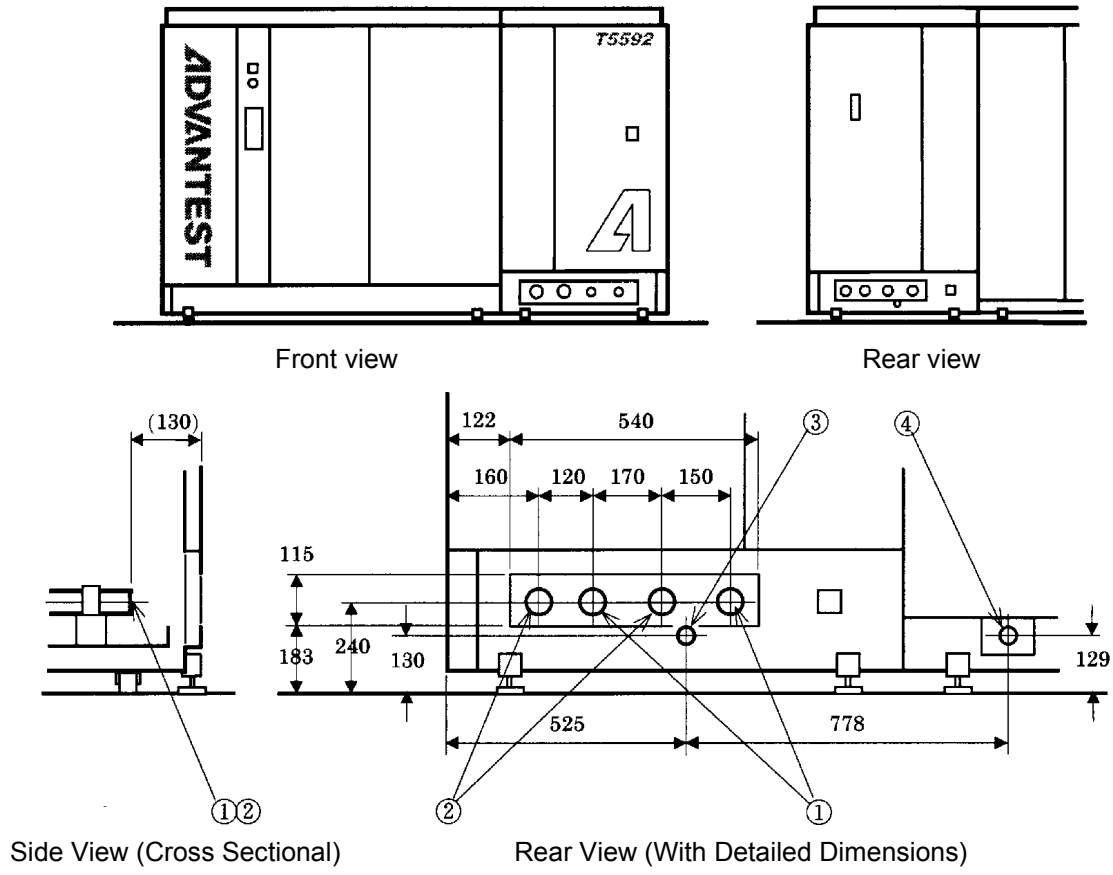


Figure 5-14 Plumbing Conditions (for the D type chiller)

(2) Plumbing Work

- All plumbing works need to be done by the customer.
- Install a 100-mesh strainer just after the cooling water inlet.
- The cooling water may cause condensation on the pipe surface, depending on the temperature of the water. Because of this, protect the plumbing from the affects of the surrounding air when necessary.
- If water leaks inside the chiller, drain the water from the chiller.
- Fluorinert may be mixed with the cooling water in the drainpipe. Because of this reason, install a valve outside the drain outlet so that the mixture of Fluorinert and cooling water is not drained directly to the effluent treatment facility.
- Install a thermometer, pressure gage and flowmeter so that the cooling water status can be monitored.
- When the test system is stopped, the inlet valve shuts the cooling water off so that the cooling water cannot flow into the chiller. The cooling water supply equipment has to operate correctly when the valve is closed.

Figure 5-15 shows an example of how the pipes are installed.

<D type chiller plumbing example >

When cooling water of 12 °C or lower is supplied, only a pair of inlet and outlet pipes can be used well enough.

However, to use only a pair of inlet and outlet pipes, connect the inlet pipe to the left port.

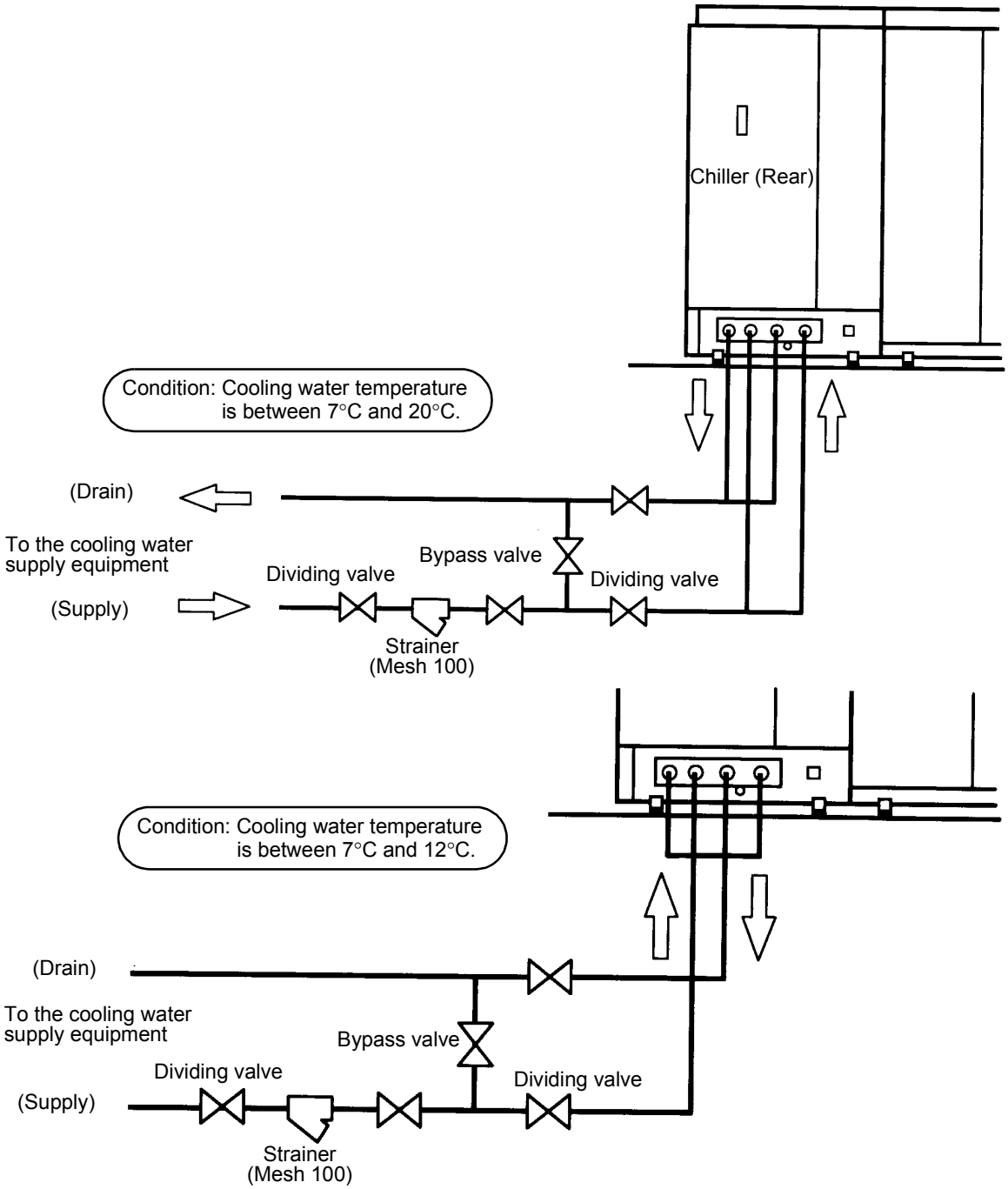


Figure 5-15 Cooling Water Plumbing Example (for the D type chiller)

<S type chiller>

(1) Plumbing conditions

The pluming positions and sizes used for the S type chiller are listed below.

① Cooling water inlet (with a valve) One position
Female taper pipe thread: Rc1 1/4 (ISO 7/1 PT 1 1/4 compliant)

② Cooling water outlet (with a valve) One position
Female taper pipe thread: Rc1 1/4 (ISO 7/1 PT 1 1/4 compliant)

③ Drain for the chiller (with a plug) One position
Female taper pipe thread: Rc 1/2 (ISO 7/1 PT 1/2 compliant)

④ Drain for the mainframe (with a plug) One position
Female taper pipe thread: Rc 1/2 (ISO 7/1 PT 1/2 compliant)

⑤ Fluorinert drain outlet (with a plug) One position
Female taper pipe thread: Rc 1/2 (ISO 7/1 PT 1/2 compliant)

⑥ Inner cooling water drain outlet (with a plug) One position
Female taper pipe thread: Rc 1/2 (ISO 7/1 PT 1/2 compliant)

⑦ Outer cooling water drain outlet (with a plug) One position
Female taper pipe thread: Rc 1/2 (ISO 7/1 PT 1/2 compliant)

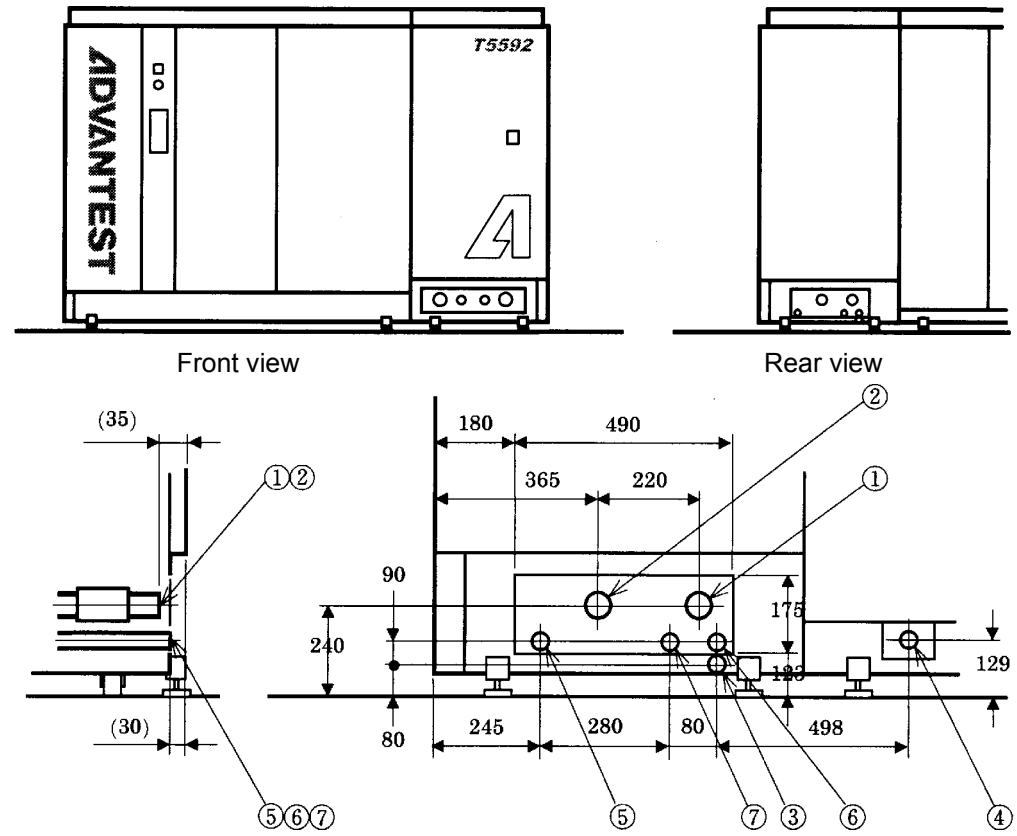


Figure 5-16 Plumbing Conditions (for the S type chiller)

(2) Plumbing Work

- All plumbing works need to be done by the customer.
- Install a 100-mesh strainer just after the cooling water inlet.
- The cooling water may cause condensation on the pipe surface, depending on the temperature of the water. Because of this, protect the plumbing from the affects of the surrounding air when necessary.
- If water leaks inside the chiller, drain the water from the chiller.
- Fluorinert may be mixed with the cooling water in the drainpipe. Because of this reason, install a valve outside the drain outlet so that the mixture of Fluorinert and cooling water is not drained directly to the effluent treatment facility.
- Install a thermometer, pressure gage and flowmeter so that the cooling water status can be monitored.
- When the test system is stopped, the inlet valve shuts the cooling water off so that the cooling water cannot flow into the chiller. The cooling water supply equipment has to operate correctly when the valve is closed.

Figure 5-17 shows an example of how the pipes are installed.

<S type chiller plumbling example>

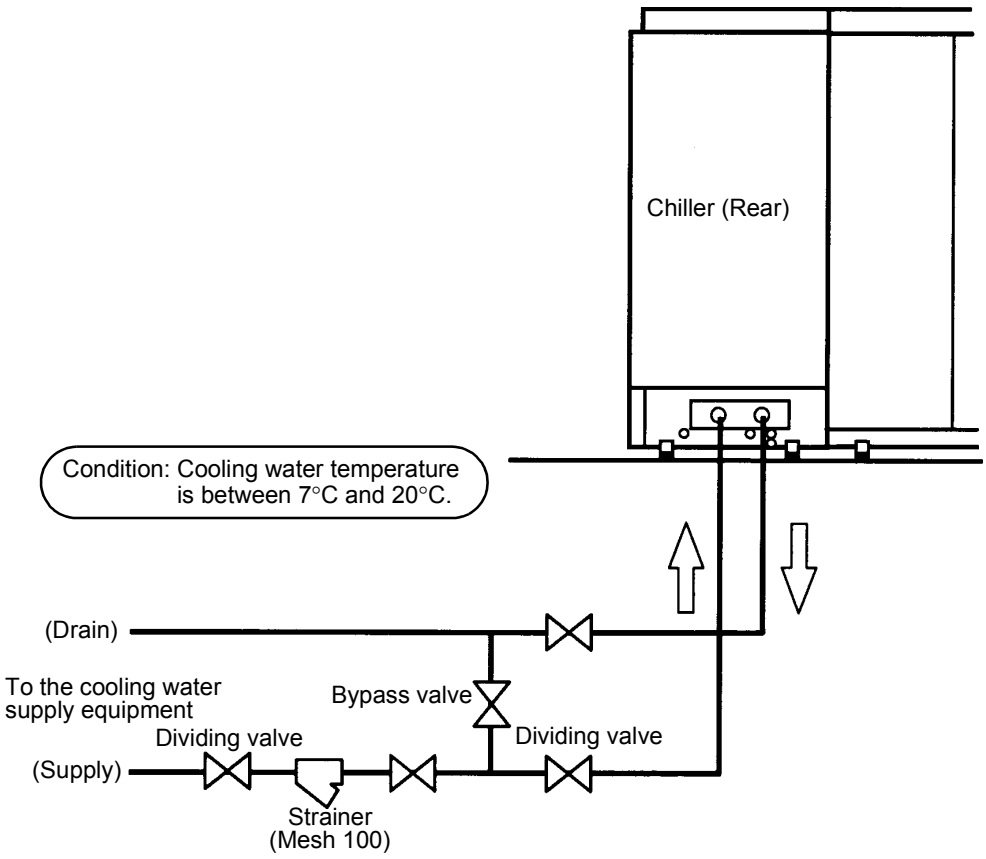


Figure 5-17 Cooling Water Plumbing Example (for the S type chiller)

5.1.12 Network Address

The T5592 memory test system should have three IP address and host names (as shown in Table 5-7). The network IP address for the environment processor are required.

Table 5-7 Factory-Set Network Address

Item	host name	IP address	Network
1	advantest	192.9.200.1	Factory network
2	asxvxhost	172.16.1.10	Local area network of tester inside
3	asxvxtarget	172.16.1.1	

- When the system is connected to the factory network, change the host name and IP address of item 1.
- Idential host name cannot be used in the factory network and items 2 and 3.
- If the IP address 172.16.0.0 is not used as the factory network ID, the IP addresses of items 2 and 3 do not need to be changed.

  If the IP address 172.16.0.0 has been used as the factory network ID, change the IP addresses for items 2 and 3.

Before you attempt to change the host name and IP address for items 2 and 3, you need to contact ADVANTEST because the tester processor settings must also be changed at the same time.

If these changes are necessary, advance notice is required in order to shorten the installation time.

5.2 Witness Test and Installation

5.2.1 Witness Inspection Procedure

If the witness inspection is required before shipment of this system from the factory, the following procedure must be used.

(1) Verification of system configuration according to acceptance specification

(2) Verification of system performance according to test certificate

(3) Test system performance test according to diagnostic programs applied by ADVANTEST

(4) Verification of carry-in conditions and installation environment

Verification of system configuration mentioned in (1) refers to a check to be conducted according to the individual manufacture specification you approved in advance.

Verification of system performance mentioned in (2) refers to a check to be conducted according to the test certificate stating the system test items and its results.

(3) is performed according to diagnostic program (PRO T5592) and diagnostic performance board. This diagnostic program is confirmed by the display of the following message.

- T5592 DIAGNOSIS ..... PASS

The check according to this diagnostic program is to be conducted for the test system which has been passed 30 minutes or more after its power source is turned on.

Test (4) is to confirm that no problems such as obstacles exist on the system transportation route and to check the installation environment and layout.

Additional requirements other than for witness test items and procedures (1) through (4) prepared by ADVANTEST should be submitted to us prior to the witness test. These requirements will be included in the witness test items when approved by us. Extra charge for the witness test by the additional requirements shall be borne by the Customer.

5.3 Installation and Acceptance

(1) The installation work includes the following:

- Delivery to specified site
- Moving into place, assembly, and adjustment
- Installation completion verification.

(2) The connection of power supply and ground lines is the customer's responsibility, it should be ready within one hour after the system has arrived.

(3) This system is transported on its attached casters, from shipping to installation site. It is essential to select an appropriate path to ensure safe carriage (be careful about stairs, cracks, width, height, rain, dust, and corrosive gases).

(4) The carriage path and the installation site must be satisfied with conditions described in 5.1 Installation Plan.

If any trouble exists, contact us beforehand.

(5) System installation is made on the basis of the layout depicted in the individual product specification.

(6) The completion of installation must be checked by following the same procedure of Section 5.2.1, and the Installation Completion Report must be created.

(7) An installation completion memo verifies that the installation and acceptance are completed.

6. DIAGNOSIS AND MAINTENANCE

6.1 System Diagnostic Programs

This system provides three system diagnostic programs:

- Self-diagnostic program for use during system startup

  The self-diagnostic program for use during system startup is used for self-diagnosis of the system processors, and is executed immediately after the system power has been turned on. The diagnosis results are displayed on the VKT. The system software will not be initiated if it fails this diagnosis check.

- System diagnostic program

  The system diagnostic program checks all of the various system functions. Its main function is to isolate faulty boards which need to be replaced.

- Peripheral diagnostic programs

  The peripheral diagnostic program checks each of the peripheral equipment functions, as well as I/O communication with the processor.

6.2 Maintenance

6.2.1 System Maintenance

The system maintenance has been designed to locate a fault board by using the system diagnostic program. The fault board can be replaced with the spare board.

6.2.2 Spare Parts

To minimize the system down time, we recommend you to purchase the following spare parts kit. The boards used on this system can be replaced with the spare parts. You can locate the fault board by using the diagnostic program, replace the fault board with a spare one, and minimize the system down time.

Spare parts kit name	Coverage of fault boards
A	Approx. 70%
A + B	Approx. 90%
A + B + C + H + I + J	Approx. 100%

Spare parts kit name	
D	Fail memory control
E	1 G AFM memory module
F	4 G AFM memory module
I	Test processor
H	256 k DBM
N	PE
K	1 M DBM

Note: The standard spare parts kit does not include in spare pin cards.

① Spare parts kit A

Name	Quantity
DC board	1
PPS board	1
SC board	1
PDS DR board	1
PDS CP board	1
DIST DR board	1
DIST CP board	1
DCMUX board	1

② Spare parts kit B

Name	Quantity
TG DIST board	1
TH DIST board	1
TG CORE board	1
PG CONT board	1
ALPG board	1
Carrying Case	1

③ Spare parts kit C

Name	Quantity
TH_IF board	1
DPU IF board	1
TG IF board	1
PS MONITOR IF board	1
TERM board (PG)	1
FTU IF board	1
PMASK board	1
CBOX IF board	1

④ Spare parts kit D

Name	Quantity
FM CONT board	1

⑤ Spare parts kit E

Name	Quantity
AFM mother board	1
1G bit AFM module	16

⑥ Spare parts kit F

Name	Quantity
AFM mother board	1
4 G AFM module	8

⑦ Spare parts kit HI

Name	Quantity
256 k DBM board	1

⑧ Spare parts kit

Name	Quantity
TP5 Base	1
TP5 CPU	1
TP5 TBUS I/F	1
PCI LVDS	1

⑨ Spare parts kit J

Name	Quantity
PE board	1
Carrying Case	1

⑩ Spare parts kit K

Name	Quantity
1 M DBM board	1

6.2.3 Chiller Maintenance

To keep the chiller operating correctly, a routine checkup is required.

(1) Daily check

Before starting the chiller, check to see the items listed below.

Coolant pressure (Fluorinert side):	High pressure: 0.75 MPa to 1.5 MPa (Note) Low pressure: 0.55 MPa to 1.0 MPa
Coolant pressure (Water side):	High pressure: 0.75 MPa to 1.5 MPa (Note) Low pressure: 0.4 MPa to 1.0 MPa
Fluorinert flow rate	45 ± 3 L/min. × 2-port piping system
Fluorinert level	27 ±1°C
Water temperature	23.5 ± 3°C
Noise and vibration	There must be no abnormal vibration or noise.
Leakage	There must be no leaks in the piping used to pass Fluorinert and water.

Tank liquid level (Fluorinert and water): The level gage indicates an appropriate level.

(2) Periodic inspection

Inspect, adjust, and clean each part of the chiller once a year. To ensure the quality of the water used in the chiller, change all of the water at least once a year.

(3) Preventive maintenance

To prevent failures and maintain the performance of the chiller, we recommend periodic overhauls including part exchanges, adjustments and an inspection. An appropriate period for this overhaul depends on your operating environment, so please contact your nearest ADVANTEST representative for more information.

Note: The S type chiller is not equipped with a coolant pressure gage.

6.2.4 Replacing Parts With Limited Life

To guarantee stable system operation, replace the parts listed below according to the estimates as shown in Table 6-1.

Note that the estimated lifespan for the parts listed below may be shortened by factors such as the environment where the system is used and how often the test system is used.

Table 6-1 Parts with Limited Life

Name	Life	Description
Unit power supply	5 years	Including capacitors
Fan motor	5 years	
Electrolytic capacitor	5 years	
Cooling water	1 year	
CD driver	5 years	
FDD	5 years	
Chiller	2 years	Pump or compressor
CRT display	5 years	
Pilot lamp (Small bulb)	6 months	Normally lit
Reed relay	100,000,000 times	In DRY mode (Shortened in WET mode)
LIF connector	10,000 times	

7. WARRANTY AND CUSTOMER SUPPORT

7.1 Warranty

This system warranty and customer support conforms to “IC Test System Warranty and Customer Support” issued by ADVANTEST CORPORATION. For the software originated by SUN Microsystems Corporation, it is necessary to make a “Software Sub-licence Agreement” between the user and ADVANTEST CORPORATION.

ADVANTEST will implement system maintenance free of charge for 12 months starting from the date of system acceptance for production defects based on the responsibility of ADVANTEST or for trouble during normal operation, excluding any other agreement between ADVANTEST and the system user.

This free-of-charge warranty is on condition that the supplied system is used properly for intended purposes, and does not apply when any modification has been made without permission of ADVANTEST and/or mishandling has occurred and/or abnormal physical or electric stress has been applied.

Also, this warranty does not apply to secondary damage of any kind in any case and/or damage caused by a factor attributable to neither ADVANTEST nor the user.

The maintenance service within the free-of-charge warrant period is implemented by maintenance work as the occasion demands.

7.2 Requirement for Preventive Maintenance

This system uses some parts for which the operating lifetime must be considered. A regular preventive maintenance program is the best means to maintain trouble-free operation.

ADVANTEST has the support resources for the user to execute the necessary preventive maintenance work.

Periodic parts replacement is required for some electronic and mechanical parts, fan motors, unit power supply, etc., in this system. If any trouble occurs in a part whose specified life has expired, performance guarantee and repair may be unavailable. For the operation lifetime of a specific part, consult with ADVANTEST as the life varies depending on various factors such as operating conditions and environment.

7.3 Recommended Equipment for Maintenance

The equipment listed below is recommended for maintenance after system installation:

(1) Tektronix model TDS 784 Digital oscilloscope with two Tek P61394A probes

(2) Tektronix model CSA803C communication signal analyzer with SD-24 sampling head

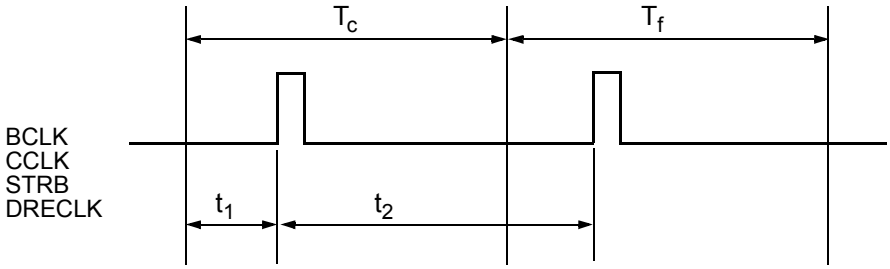
(3) Five-digit digital voltmeter with 1 mV resolution and accuracy of at least 0.01%

8. TESTER MAINFRAME SPECIFICATIONS

This chapter describes the system specifications which are valid when the system power supply is turned on and the automatic calibration is executed 30 minutes after startup of system software.

8.1 Timing Generator

8.1.1 Timing Edge Specifications



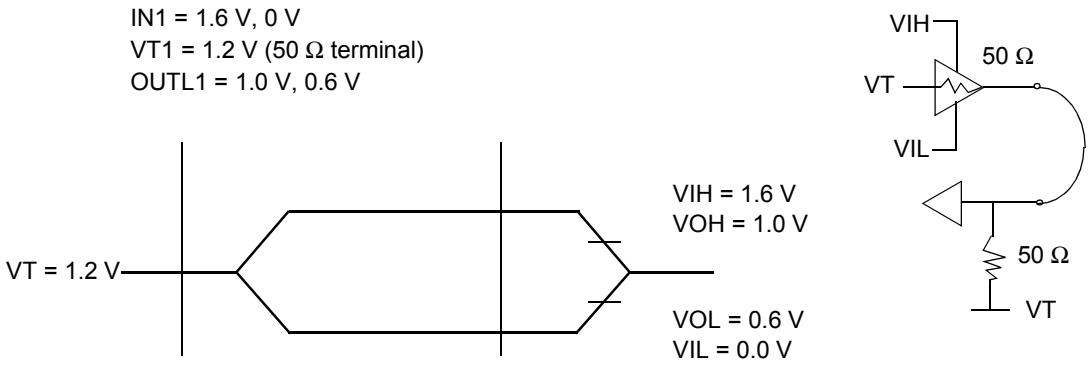
		Specification
Test rate	1WAY	7.5 ns $\leq T_c, T_f \leq$ 7.68 µs
	2WAY	3.75 ns $\leq T_c, T_f \leq$ 3.84 µs
	4WAY	1.875 ns $\leq T_c, T_f \leq$ 1.92 µs
Test rate setting resolution		14.6484375 ps
Timing edges	BCLK CCLK DRECLK STRB	960 ns $\geq t_1 \geq$ 0 ns T_c+T_f -resolution $\geq t_1$ In 1WAY operation, $t_2 \geq$ 7.5 ns In 2WAY operation, $t_2 \geq$ 3.75 ns In 4WAY operation, $t_2 \geq$ 1.875 ns
Timing edge setting resolution		14.6484375 ps

8.2 Driver Specifications

8.2.1 BiCMOS Station

Output level	V_{IH} : –1.8 V to 5.5 V V_{IL} : –2.5 V to 5 V	
Output amplitude	0.2 Vp-p to 8.0 Vp-p	(Note 3)
DC accuracy	Within ± (0.5%+10 mV)	
Driver rise time/fall time	400 ps±100 ps/0 - 1.6 V (20% to 80%)	(Note 2)
Overshoot (driver only)	Within ± (5%+30 mV)	(Note 2)
Minimum pulse width	0.9375 ns/1.6 Vp-p	(Note 2)
Driver skew	p-p 60 ps or less	(Note 2)
Output impedance	50 Ω ±5 Ω/25 mA or more, 50 Ω ±2 Ω/25 mA or less	
Maximum output current	At high level: Source current Sink current At low level: Source current Sink current	 40 mA 40 mA 40 mA 40 mA
I/O switching accuracy (on time, off time)	p-p 400 ps	(Note 1)
Minimum ON time during I/O	2.0 ns	(Note 1)
Minimum OFF time during I/O	2.0 ns	(Note 1)

Note 1: Condition for measuring the I/O change accuracy



Note 2: Under the load condition of a 25 cm long, 50 Ω coaxial cable.

Note 3: The AC output current is ± 55 mA or less.

8.3 Comparator Specifications

8.3.1 BiCMOS Station

Equivalent rise time	300 ps/1.6 V (20% to 80%) (Note 2)
Comparator skew	pp 60 ps or less (Note 2)
Input voltage range	–2.5 V to 5.5 V
Reference voltage accuracy	Within ±(0.5%+10mV)

Note 1: On the T5592 system, the I/O dead band is not generated because it adopts the DTL mode.

Note 2: Under the load condition of a 25 cm long, 50 Ω coaxial cable and 50 Ω termination.

8.4 Dynamic Clamp Specifications

8.4.1 BiCMOS Station

Clamp voltage level	High: –1.7V to 5.9V Low: –2.8V to 5.2V
Clamp voltage precision	± (5.0% + 200 mV) at 8 mA
Voltage resolution	16 mV
Clamp DC current	High: –20 mA Low: 20 mA

8.5 Terminator Specifications

8.5.1 BiCMOS Station

Item		Specification
Resistor accuracy		50 Ω±5 Ω/>20 mA, 50 Ω±2 Ω/≤20 m
Pull-up voltage range		–2.5 V to 5.5 V (Note)
Pull-up voltage accuracy		±(0.5%+10 mV)
Pull-up voltage resolution		2 mV
Maximum Current	Dr side	±25 mA
	Cp side	±40 mA

Note : ***The terminating voltage (V_{TT}) is limited within the following range:***
–2.0 V ≤ Input voltage – VT ≤ 2.0 V

8.6 DC Parametric Test Unit Specifications

8.6.1 Voltage Forcing/Current Measurement (VSIM)

Output value specified on a performance board.

(1) Programmable Voltages

Setting voltage range	Output voltage range	Resolution	Maximum current (*)
10V	-6.000V to +10.000V	2 mV	±80 mA

**** The maximum current is limited by the current measurement range and the current limit.***

Setting voltage range	Program accuracy (10 to 100% full scale)
10V	±(0.1% + 4 mV + 2 mV / 10 mA)

(2) Current Measurements

Current measurement range	Measurement range	Resolution	Measurement accuracy (10 to 100% of full scale)
8μA	0 to ±7.998μA	2 nA	±(0.5% + 6 nA + 0.5 nA/V)
80μA	0 to ±79.98μA	20 nA	±(0.2% + 40 nA + 5 nA/V)
800μA	0 to ±799.8μA	200 nA	±(0.2% + 0.4 μA + 50 nA/V)
8mA	0 to ±7.998mA	2 μA	±(0.2% + 4 μA + 0.5 μA/V)
80mA	0 to ±79.98mA	20 μA	±(0.5% + 60 μA + 5 μA/V)

(3) Current limits (for positive and negative values)

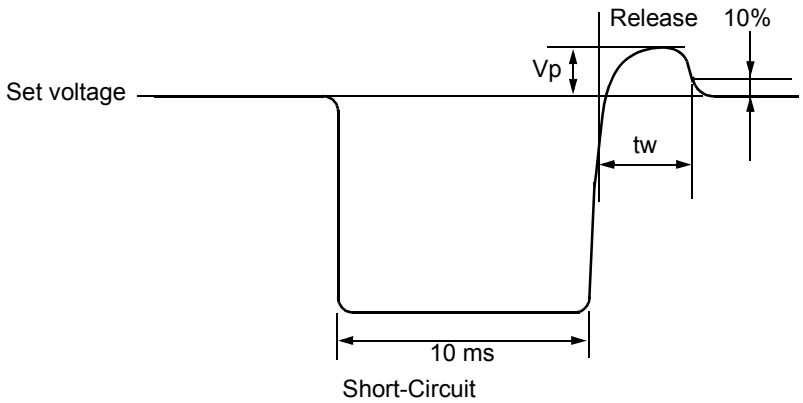
Current measurement range	Setting range	Resolution	Current limit accuracy	
8μA	±0.999mA constant*	—	Positive	+2 mA
			Negative	-2 mA
80μA	±0.999mA constant*	—	Positive	+2 mA
			Negative	-2 mA
800μA	±0.999mA constant*	—	Positive	+2 mA
			Negative	-2 mA
8mA	±(0.999mA to 8.0253mA) constant*	33.3 μA	Positive	+(20% + 2 mA) to 0 A
			Negative	-(20% + 2 mA) to 0 A
80mA	±(9.99mA – 80.253mA)	333 μA	Positive	+(20% + 20 mA) to 0 A
			Negative	-(20% + 20 mA) to 0 A

* ***Non-programmable***

(4) Output Short-Circuit to Open Characteristics

Current measurement range	Peak voltage (v_p)	Recovery time (tw) (*1)
8μA to 80mA	1 V	2 ms or less

1 The recovery time is the time required to reach the set value ±10% when short-circuit and open are repeated at 10 ms intervals with no load other than the short-circuit load.



8.6.2 Current Forcing/Voltage Measurement (ISVM)

Output value specified on a performance board.

(1) Programmable Current

Setting current range	Output current range	Resolution	Maximum output voltage (*)	Output impedance on reference off
80μA	0 to ± 80.00μA	20 nA	-6.262 V to +10.437 V	470 KΩ ± 10%
800μA	0 to ± 800.0μA	200 nA		470 KΩ ± 10%
8mA	0 to ± 8.000mA	2 μA		470 KΩ ± 10%
80mA	0 to ± 80.00mA	20 μA		1 KΩ ± 20%

* ***The maximum output voltage is limited by the current measurement range and the voltage limit.***

Setting current range	Program accuracy (10 to 100% of full scale)
80μA	±(0.2% + 20 nA + 100 nA/V)
800μA	±(0.2% + 0.2 μA + 1 μA/V)
8mA	±(0.2% + 2 μA + 10 μA/V)
80mA	±(0.5% + 40 μA + 100 μA/V)

(2) Voltage measurements

Voltage measurement range	Measurement range	Resolution	Measurement accuracy
10V	-5.996V to +9.998V	2 mV	±(0.1% + 4 mV + 2 mV/10 mA)

(3) Voltage Limit

Setting range	Resolution	Accuracy	Minimum setting voltage
-6.262V to + 10.437V	42.6 mV	±0.3 V	±0.596 V

The maximum voltage limit is about 1.25 times the full-scale voltage range.

8.6.3 Maximum Load Capacity (VSIM and ISVM)

Voltage Range / Current Range	10 V
8μA	100 pF
80μA	1000 pF
800μA	1000 pF
8mA	0.01 μF
80mA	0.1 μF

The maximum load capacity guarantees 10% of the set value of overshoot/undershoot due to reference ON/OFF or 0.5 V, whichever is greater, when the maximum load capacity is connected.

8.6.4 Voltage Measurement (MVM)

Voltage measurement range	Voltage measurement range	Measurement resolution	Measurement accuracy	Input impedance
8V	-5.998V to +9.998V	2 mV	±(0.1%+4 mV)	10 MΩ or more

8.6.5 VSIM Settling Time

Forcing Voltage Range	Current Measurement Range	Deviation of the Measured Values from the Final Value		
		Within 1% of f.s.	Within 0.1% of f.s.	Within 1% of 1/10 f.s.
10V	8µA	5 ms	10 ms	10 ms
	80µA	0.4 ms	0.5 ms	0.5 ms
	800µA	0.2 ms	0.3 ms	0.3 ms
	8mA			
	80mA			

Load condition: Resistance + Capacitance (100 pF)

8.6.6 ISVM Settling Time

IS		VM			
IS range	Setting value	1.0 V		10 V	
		1%	0.1%	1%	0.1%
80µA	8 µA	1	1.5	6	12
	80 µA	0.2	0.3	0.5	0.8
800µA	80 µA	0.3	0.5	1.5	2
	800 µA	0.2	0.3	0.2	0.3
8mA	800 µA	0.2	0.3	0.8	1.5
	8 mA	0.2	0.3	0.2	0.3
80mA	8 mA	0.2	0.3	0.8	1.5
	80 mA	0.2	0.3	0.2	0.3

Settling time: Maximum time (ms) until the deviation of the measured value from the final value comes within 0.1% or 1%

Load condition: Resistance + capacitance (100 pF)

The voltage level for the VM at 0.16 V and a deviation of 0.1% are below measurement resolution; time values are omitted from this table.

8.7 Device Power Supply Specifications

8.7.1 Voltage Forcing/Current Measurement (VS)

(1) Programmable Voltage

Setting voltage range	Output voltage range	Resolution	Programmable accuracy	Maximum output current *1
16V	-6V to +16V	2 mV	±(0.1% + 4 mV)	400 mA
5V	0V to +5V	2 mV	±(0.1% + 4 mV)	800 mA

1 The maximum output current depends on the current limit and current measurement range.

(2) Current Limit (Positive and negative current can be set individually.)

Current measurement range	Setting voltage value	Setting range	Setting resolution	Current limit accuracy
4μA to 4mA	-3 V ≤ VS ≤ +8 V	0 to 400mA	5 mA	+(15% + 40 mA) to 0 A
4μA to 4mA	+8 V < VS ≤ +13 V	0 to 200mA	5 mA	+(15% + 40 mA) to 0 A
80mA	-6 V ≤ VS < -3 V +13 V < VS ≤ +16 V	0 to 80mA	5 mA	+(15% + 40 mA) to 0 A
80mA	-3 V ≤ VS ≤ +8 V	0 to 400mA	5 mA	+(15% + 40 mA) to 0 A
80mA	+8 V < VS ≤ +13 V	0 to 200mA	5 mA	+(15% + 40 mA) to 0 A
800mA	-6 V ≤ VS <v0 V +5 V < VS ≤ +13 V	0 to 400mA	5 mA	+(15% + 40 mA) to 0 A
800mA	0 V ≤ VS ≤ +5 V	0 to 800mA	5 mA	+(15% + 40 mA) to 0 A
800mA	+13 V < VS ≤ +16 V	0 to 200mA	5 mA	+(15% + 40 mA) to 0 A

(3) Current Measurement

Current measure-ment range	Setting range	Setting resolution	Measurement accuracy	Maximum output current *1	Maximum capacity load
4μA	0 to ±3.998μA	2 nA	±(0.5% +10 nA + 1 nA/V)	400 mA	1 μF
40μA	0 to ±39.98μA	20 nA	±(0.5% +60 nA + 10 nA/V)	400 mA	1 μF
400μA	0 to ±399.8μA	200 nA	±(0.5% +600 nA + 100 nA/V)	400 mA	1 μF
4mA	0 to ±3.998mA	2 μA	±(0.5% +6 μA + 1 μA/V)	400 mA	1 μF
80mA	0 to ±79.96mA	40 μA	±(0.5% +120 μA + 20 μA/V)	400 mA	10 μF
800mA	0 to ±799.6mA	400 μA	±(0.5% +1.2 mA + 200 μA/V)	800 mA	33 μF

1 Determined depending on limit current value and setting voltage value.

Control can branch conditionally according to the operating conditions of the current limit circuit. If the load current is within limit, the auto-range measurement can be performed without using the reference ON/OFF.

(4) Maximum Capacitance Load

Current measurement range	Without C setting	With C1 setting	With C2 setting
4μA	0.1 μF	0.1 μF	1 μF
40μA	0.1 μF	0.1 μF	1 μF
400μA	1 μF	1 μF	1 μF
4mA	1 μF	1 μF	1 μF
80mA	10 μF	10 μF	10 μF
800mA	33 μF	33 μF	33 μF

The maximum load capacity guarantees 10% of the set value of overshoot/undershoot due to reference ON/OFF or 0.5 V, whichever is greater, when the maximum load capacity is connected.

(5) Slew Rate

Setting voltage range	Setting range	Setting resolution	Program accuracy
16V	15.6μS/V to 1996.8μS/V	7.8 μV	±20%
5V	15.6μS/V to 1996.8μS/V	7.8 μV	±20%

(6) VSIM Settling Time

Current measurement range	Difference between measurement and final values (1% of measurement value or 20 counts, which is greater)			
	Load capacity			
	No load	0.1 μF	1 μF	10 μF
4μA	6 ms	12 ms	100 ms	
40μA	3 ms	5 ms	12 ms	
400μA	5 ms			
4mA	3 ms			
80mA	3 ms			
800mA	3 ms			

8.7.2 Voltage Forcing/Current Measurement (parallel connection)

The n means the number of channel in the parallel connection. FSR (Full Scale Range) means the range of current measurement in the parallel connection.

For example, FSR in the 2 channel parallel connection is 1.6 A.

(1) Programmable Voltage

Setting voltage range	Output voltage range	Setting resolution	Program precision	Maximum output current *2
16V	-6V to +16V	2 mV	±(0.1% + 22 mV *1)	n × 400 mA
5V	0V to +5V	2 mV	±(0.1% + 22 mV *1)	n × 800 mA

1 Changes depend on load current. (This is the value when max. output current.)

2 The maximum output current depends on the current limit and current measurement range.

(2) Current Limit (Positive and negative current can be set individually.)

Current measurement range	Setting voltage value	Setting range	Setting resolution	Current limit accuracy
4μA to M80mA	Unusable			
n × 800mA	-6 V ≤ VS < 0 V +5 V < VS ≤ +13 V	n × 400mA is fixed	n × 5 mA	+(15% of FSR + n × 40 mA) to 0 A
n × 800mA	0 V ≤ VS ≤ +5 V	n × 800mA is fixed	n × 5 mA	+(15% of FSR + n × 40 mA) to 0 A
n × 800mA	+13 V < VS ≤ +16 V	n × 200mA is fixed	n × 5 mA	+(15% of FSR + n × 40 mA) to 0 A

(3) Current Measurement

Current measurement range	Measurement range	Measure-ment resolution	Measurement accuracy	Maximum output current *1	Maximum capacity load
4μA to M80mA	Unusable				
n × 800mA	0 to ± n × 799.6mA	n × 400 μA	±(0.5% of FSR +n × 1.2 mA +n × 200 μA/V)	n × 800 mA	n × 33 μF

1 Determined depending on setting voltage value.

Control can branch conditionally according to the operating conditions of the current limit circuit.

(4) Measurement Capacitance

Current measurement range	Without C1 setting	With C1 setting
4μA to 80mA	Unusable	
n × 800mA	n × 33 μF	n × 33 μF

The maximum load capacity guarantees 10% of the set value of overshoot/undershoot due to reference ON/OFF or 0.5 V, whichever is greater, when the maximum load capacity is connected.

(5) Slew Rate

Setting voltage range	Setting range	Setting resolution	Program accuracy
16V	15.6μS/V to 1996.8μS/V	7.8 μS/V	±20%
5V	15.6μS/V to 1996.8μS/V	7.8 μS/V	±20%

8.7.3 Voltage Forcing/Voltage Measurement (VSVM)

(1) Programmable Voltage

Set voltage range	Setting range	Resolution	Setting accuracy	Maximum Output current	Output impedance
16V	-6V to +16V	2 mV	±(0.1% + 10 mV)	20 mA	1 KΩ±10%

(2) Voltage Measurement Range

Voltage measurement range	Measurement range	Measurement resolution	Measurement accuracy	Output impedance
16V	-5.996V to +15.996V	4 mV	±(0.2%+12 mV)	10 MΩ or more

8.7.4 Voltage Measurement (MVM)

(1) Voltage Measurement

Voltage measurement range	Measurement range	Measurement resolution	Measurement accuracy	Input impedance
16V	-5.996V to +15.996V	4 mV	±(0.2% + 12 mV)	10 MΩ or more

8.7.5 Failure Detect

Alarm name	Detecting limit	Detecting timing	Correspondence
Kelvin connection abnormality	Forced line voltage drop is more than 2 V.	All time (interrupt)	System error
Guard drive abnor-mality	Guard line current is more than 5 mA.	MEAS statement	Runtime error
Current limiter start	Current limiter circuit start	MEAS statement	Conditional branch

8.7.6 Filter for Measurement

It is possible to set the -20 dB/dec lowpass filter.

Filter setting	Cut off frequency	Setting accuracy
Off	17.5 kHz	±20%
FLT1	1.59 kHz	±20%
FLT2	173 Hz	±20%
FLT3	16 Hz	±20%

8.7.7 Measurement Function for Average Current

Sampling rate: 1 ms (fix)

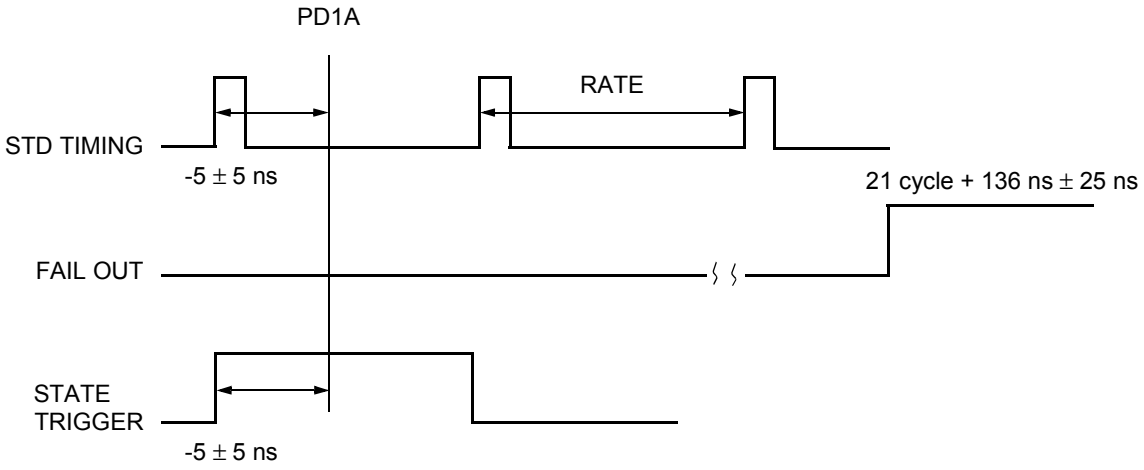
Stop timer: 1 second max.

Operation mode	Measurement Start/Stop
1	Start by Test statement/Stop by the numbers of averaging time.
2	Start from the Pattern Program/Stop from the Pattern Program.
3	Start from the Pattern Program/Stop by the numbers of averaging time.

8.8 Trigger Panel Output Timing

Output connector	Timing	Condition
STD TIMING	-5 ± 5 ns	PD1A on performance board: 0 to 3 V (50%)
FAIL OUT	21 cycle + 136 ns ± 25 ns	
STATE TRIGGER	-5 ± 5 ns	

Timing chart



Note: ***In 2 WAY interleave operation, the trigger signal is output only to the cycle on the 1st side.***

8.9 Utility Power Supply

Voltage accuracy	RLVCC	5.1 V ± 0.4 V
	PBVCC	5.1 V ± 0.4 V
Maximum current	RLVCC	Total 10 A
	PBVCC	

9. COMPUTING SYSTEM SPECIFICATIONS

Note that the specifications of the computing system given in this chapter are subject to change without notice.

9.1 Processor

9.1.1 Environment Processor

Module Name:	Ultra5
CPU:	64-bit processor/UltraSPARC-IIi 256 kB external cache memory
Main Memory:	128 MByte memory Expandable up to 512 MByte as an option
I/O:	Serial Interface Port (RS-423/RS-232C) × 2 Ethernet/Fast Ethernet standard twisted pair Parallel interface port
Graphic Monitor	
V0105B:	1152 × 900 Pixel, 21-inch Color Monitor
V0106B:	1152 × 900 Pixel, 17-inch Color Monitor
Graphic accelerator:	8/24-bit color, PGX
Keyboard:	North American Universal
Mouse:	Optomechanical method (exclusive pat), 3-selectable button

9.1.2 Tester Processor

Module Name:	TP5
CPU:	32-bit processor for data and instructions (24-bit addressing)
Main Memory:	8 MByte memory
Tester Control Bus:	10 MByte per second data rate

Note: ***Under the situation of a strong electromagnetic field which exceeds 3 V/m, the picture of the Monitor may flicker slightly and at even high field strength the monitor shutdown automatically.***
In such a case, please change the monitor location.

9.2 Peripheral Equipment

(1) Hard disk (Standard)

Memory capacity:	8 GByte / 9 GByte
Drive size:	3.5-inch
Interface specifications:	Expansion IDE (EIDE)
Average random seek time: (read/write)	9 ms (8 GByte) / 9.5 ms (9 GByte)
Number of revolutions:	5400 rpm (8 GByte) / 7200 rpm (9 Byte)

(2) Hard Disk (External option)

Memory capacity:	9.1 GByte / 18.2 GByte
Drive size:	3.5-inch
Interface specifications:	Ultra SCSI
Average seek time (read/write)	7.4 ms/8.2 ms (9.1 GByte), 8.0 ms/9.0 ms (18.2 GByte)
Number of revolutions:	7200 rpm

(3) 1/4-inch cartridge tape device (option)

Model name:	H3-6616B
Maximum capacity:	4 GByte (normal mode)/8 GByte (compression mode)
Read/write speed:	76 IPS
Recording density:	62000 FRPI
Tape length:	1500 feet
Write format type:	QIC4GB
Compatibility with read:	QIC150, QIC2GB, QIC4GB

(4) CD-ROM drive device (option)

Media size:	5.25-inch
Disk capacity (format):	527.3 MByte (mode1) 601.5 MByte (mode2)
User data block size:	2048-Byte (mode1) 2336-Byte (mode2)
Drive performance:	32 speed drive

(5) 3.5-inch floppy disk (standard)

Floppy Media size:	3.5-inch
Memory capacity:	720 k, 1.2 M, 1.44 MByte (format)
Number of sectors:	9, 8, 18 sectors/track
Sector capacity:	512, 1024 Byte/sec
Revolution speed:	300, 360 rpm

(6) Color Laser Printer (Optional)

Product Name:	V0225
Print Resolution:	1200 dpi (in black), 600 dpi (in color)
Print Speed:	16 pages per minute (in black) 5 pages per minute (in color)
Memory:	32 MB
Paper Sizes:	A4
Fonts:	136 fonts
Print Language:	Adobe PostScript 3
Connectivity:	Ethernet

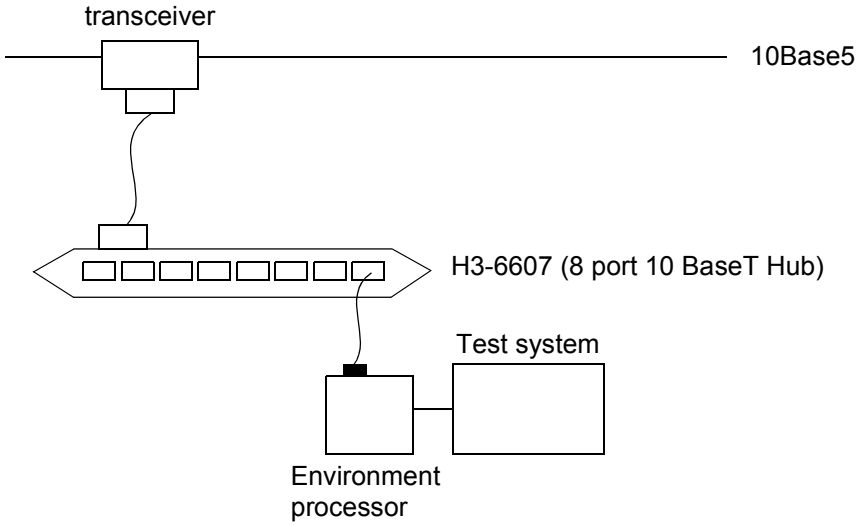
Note: The test systems can not provide power for the color laser printer. Please prepare 100 VAC outlets to operate the printers.

9.3 External Computer Interface

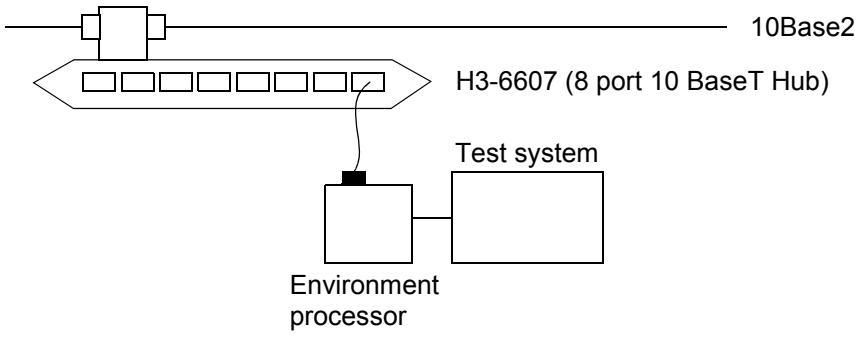
Ethernet is provided.

Ethernet and Fast Ethernet (twisted pair cables 10BaseT/100BaseT) are available.

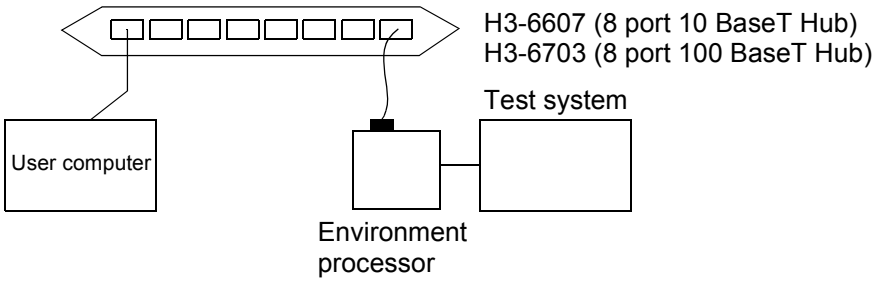
(1) When communicating with external computers through 10 Base5



(2) When communicating with external computers through 10 Base2



(3) When communicating with external computers through 100BaseT



10. SYSTEM CONFIGURATION

- Computing System

Table 10-1 System Configuration

	Ultra 5	
Item	Standard	Option
Environment Processor Memory	128 MByte	Extended up to 512 MByte
Graphic Display Terminal	1 (21” or 17” color)	——
Hard Disk	1 (8 GByte)	9.1 G / 18.2 GByte, a maximum of 2 hard disk
CD-ROM Drive Device	1	——
Cartridge Magnetic Tape Device	0	1
Ethernet/Fast Ethernet (10/100 BaseT)	1 port	1 port
Test Processor Memory	8 MByte	——
GPIB Interface	0	1

10. SYSTEM CONFIGURATION

- T5592 main frame

Configuration		Q'ty		Conditions
		Standard	Max	
ALPG	X Address	16 bits		
	Y Address	16 bits		
	Data	18 bits × 2		
	Instruction Memory	1 K word		
	Sub ALPG	Installed		Max 133 MHz, Synchronous
Timing Generator	BCLK	1 edge/pin		Max 128
	CCLK	1 edge/pin		Max 128
	DRECLK (DREL , DRET)	2 edge/IO pin		Max 256
	STRB	2 edge/IO pin		Max 128
	Timing Set	16 TS		
FM	Address Fail Memory	0	8 G bits	1 G AFM Module
		0	32 G bits	4 G AFM Module
Data Buffer Memory (PPAT, PCPE, PDRE)		96 bits×256 k (96 bits×1 M)		2 WAY; 512 k (2 M) 4 WAY; 1 M (4 M)
DC Test Unit		32 (16) [16]		/STN ( ): half [ ]: quarter
800 mA PPS		128 CH (64 CH) [64 CH]	128 CH (128 CH) [128 CH]	/STN ( ): half [ ]: quarter
Driver Output Voltage Vih, Vil		16 groups		
Comparator Comparison Voltage Voh, Vol		16 groups		
Pull-up Voltage Vt		16 groups		
Programmable Load Ioh, Iol		16 groups		
Handler or Prober GP-IB Interface		1		
EMO switch (without key)		1	2	
Test Head Number		1	2	
Test Head Cabinet		0	1	/STN
Trigger Panel		1		/STN

Configuration	Q'ty		Conditions
	Standard	Max	
Control Box	1		/STN

- T5592 channel

Configuration		Full	Half	Quarter	Conditions
Format Control	Driver Channel	72	72	36	
	I/O Channel	96	96	48	
Test Station	Driver Channel	576	288	144	/STN
	I/O Channel	768	384	192	/STN
	Driver Channel (For clock generation)	96	48	24	/STN

- Others

Configuration	Q'ty		Conditions
	Standard	Max	
Manual	1 set	*	
Extender Card	0	1 set	
Accessories	1 set		
Test Report	1 set		