%JOB_START - Beginning CUB Calibration test on slot 18 at 11:29:14 AM on 1/17/2020
Workbook Rev V7.60.40IP02 DC1116 IG-XL Version: 3.50.40IP02 DIB: P/N 51745600 S/N xxxxxxx Rev 0901A

%INFO - ----------
%INFO - System IP750_ (IP750EX)
%INFO - IG-XL 3.50.40IP02, Build: 04.13.11.20.00
%INFO - Maintenance 7.60.40IP02, Build: 04.18.11.02.09
%INFO - ----------
- Starting Channel Drive Levels: Vih Vil
- Starting Channel Compare Levels: Voh Vol
- Finished Channel Calibration

%JOB_END - ****PASSED**** CUB Calibration of slot 18 (S/N:) at 11:29:14 AM

%JOB_START - Beginning Channel_Board_DIB Calibration test on slot(s) 0,1 at 11:29:27 AM on 1/17/2020
Workbook Rev V7.60.40IP02 DC1116 IG-XL Version: 3.50.40IP02 DIB: P/N 51745600 S/N xxxxxxx Rev 0901A

%INFO - ----------
%INFO - System IP750_ (IP750EX)
%INFO - IG-XL 3.50.40IP02, Build: 04.13.11.20.00
%INFO - Maintenance 7.60.40IP02, Build: 04.18.11.02.09
%INFO - ----------
- Starting DC Calibration on slot 0
- Systemwide functionality and continuity to slot 0
- Starting dib_test
- Temperature at PE Ch00 is 38 deg C
- Temperature at PE Ch60 is 37 deg C
- Temperature at TG Ch60 is 26 deg C
- Temperature at TG Ch00 is 48 deg C
- Starting BPMU Force Voltage
- Starting Bpmu Clamp Voltage
- Starting Bpmu Measure Voltage
- Starting Bpmu Measure Current
- Starting Bpmu Force current
- Starting Bpmu Limit current
- Starting Channel Drive Levels: Vih Vil
- Starting Channel Drive Levels: VT50ohm
- Starting Channel Compare Levels: Voh Vol
- Starting Channel Clamps: Vch Vcl
- Starting Channel Loads: Ioh Iol
- Starting Channel Load Threshold: Vt
- Starting HV Channel Drive Levels
- Starting HV Channel Drive Current
- Starting FHV Channel Drive Levels
- Ppmu Mi Warmup 11:31:34 AM
- Ppmu Mi Warmup 11:31:34 AM
- Starting Ppmu Force Voltage
- Starting Ppmu Measure Voltage
- Starting Ppmu Force Current Ppmu Force 200ua

- Starting Ppmu Force Current Ppmu Force 2ma
- Starting Ppmu Force Current Ppmu Force 50ma
- Starting Ppmu Force Current Ppmu Force 20ua
- Starting Ppmu Measure 2ma
- Continuing Ppmu Measure Current chan 15
- Continuing Ppmu Measure Current chan 31
- Continuing Ppmu Measure Current chan 47
- Continuing Ppmu Measure Current chan 63
- Starting Ppmu Measure 200ua
- Continuing Ppmu Measure Current chan 15
- Continuing Ppmu Measure Current chan 31
- Continuing Ppmu Measure Current chan 47
- Continuing Ppmu Measure Current chan 63
- Starting Ppmu Measure 20ua
- Continuing Ppmu Measure Current chan 15
- Continuing Ppmu Measure Current chan 31
- Continuing Ppmu Measure Current chan 47
- Continuing Ppmu Measure Current chan 63
- Starting Ppmu Measure 2ua
- Continuing Ppmu Measure Current chan 15
- Continuing Ppmu Measure Current chan 31
- Continuing Ppmu Measure Current chan 47
- Continuing Ppmu Measure Current chan 63
- Starting Ppmu Measure 50ma
- Continuing Ppmu Measure Current chan 15
- Continuing Ppmu Measure Current chan 31
- Continuing Ppmu Measure Current chan 47
- Continuing Ppmu Measure Current chan 63
- Finished Channel Calibration
- Finished DC Calibration on slot 0
- Starting DC Calibration on slot 1
- Systemwide functionality and continuity to slot 1
- Starting dib_test
- Temperature at PE Ch00 is 36 deg C
- Temperature at PE Ch60 is 36 deg C
- Temperature at TG Ch60 is 25 deg C
- Temperature at TG Ch00 is 45 deg C
- Starting BPMU Force Voltage
- Starting Bpmu Clamp Voltage
- Starting Bpmu Measure Voltage
- Starting Bpmu Measure Current
- Starting Bpmu Force current
- Starting Bpmu Limit current
- Starting Channel Drive Levels: Vih Vil
- Starting Channel Drive Levels: VT50ohm
- Starting Channel Compare Levels: Voh Vol
- Starting Channel Clamps: Vch Vcl
- Starting Channel Loads: Ioh Iol
- Starting Channel Load Threshold: Vt
- Starting HV Channel Drive Levels
- Starting HV Channel Drive Current
- Starting FHV Channel Drive Levels

- Ppmu Mi Warmup 11:37:11 AM
- Ppmu Mi Warmup 11:37:11 AM
- Starting Ppmu Force Voltage
- Starting Ppmu Measure Voltage
- Starting Ppmu Force Current Ppmu Force 200ua
- Starting Ppmu Force Current Ppmu Force 2ma
- Starting Ppmu Force Current Ppmu Force 50ma
- Starting Ppmu Force Current Ppmu Force 20ua
- Starting Ppmu Measure 2ma
- Continuing Ppmu Measure Current chan 79
- Continuing Ppmu Measure Current chan 95
- Continuing Ppmu Measure Current chan 111
- Continuing Ppmu Measure Current chan 127
- Starting Ppmu Measure 200ua
- Continuing Ppmu Measure Current chan 79
- Continuing Ppmu Measure Current chan 95
- Continuing Ppmu Measure Current chan 111
- Continuing Ppmu Measure Current chan 127
- Starting Ppmu Measure 20ua
- Continuing Ppmu Measure Current chan 79
- Continuing Ppmu Measure Current chan 95
- Continuing Ppmu Measure Current chan 111
- Continuing Ppmu Measure Current chan 127
- Starting Ppmu Measure 2ua
- Continuing Ppmu Measure Current chan 79
- Continuing Ppmu Measure Current chan 95
- Continuing Ppmu Measure Current chan 111
- Continuing Ppmu Measure Current chan 127
- Starting Ppmu Measure 50ma
- Continuing Ppmu Measure Current chan 79
- Continuing Ppmu Measure Current chan 95
- Continuing Ppmu Measure Current chan 111
- Continuing Ppmu Measure Current chan 127
- Finished Channel Calibration
- Finished DC Calibration on slot 1

%JOB_END - ****PASSED**** Channel_Board_DIB Calibration of slot(s) 0, 1 at 11:40:41 AM
- PASS slot 0 (S/N)
- PASS slot 1 (S/N)

%JOB_START - Beginning DPS_DIB Calibration test on slot 22 at 11:40:54 AM on 1/17/2020
Workbook Rev V7.60.40IP02 DC1116 IG-XL Version: 3.50.40IP02 DIB: P/N 51745600
S/N xxxxxxx Rev 0901A

%INFO - ----------
%INFO - System IP750_ (IP750EX)
%INFO - IG-XL 3.50.40IP02, Build: 04.13.11.20.00
%INFO - Maintenance 7.60.40IP02, Build: 04.18.11.02.09
%INFO - ----------
- Starting DPS Calibration on slot 22

- Calibrating DPS Voltage on slot 22

- Calibrating DPS Current Limit on slot 22
- Calibrating DPS Current Measure (50uA Range) on slot 22
- Calibrating DPS Current Measure (500uA Range) on slot 22
- Calibrating DPS Current Measure (10mA Range) on slot 22
- Calibrating DPS Current Measure (100mA Range) on slot 22
- Calibrating DPS Current Measure (1A Range) on slot 22

- Finished DPS Calibration on slot 22

%JOB_END - ****PASSED**** DPS_DIB Calibration of slot 22 (S/N:) at 11:41:17 AM

%JOB_START - Beginning APMU Calibration test on slot 5 at 11:41:30 AM on 1/17/2020
Workbook Rev V7.60.40IP02 DC1116 IG-XL Version: 3.50.40IP02 DIB: P/N 51745600 S/N xxxxxxx Rev 0901A

%INFO - ----------
%INFO - System IP750_ (IP750EX)
%INFO - IG-XL 3.50.40IP02, Build: 04.13.11.20.00
%INFO - Maintenance 7.60.40IP02, Build: 04.18.11.02.09
%INFO - ----------
- Starting APMU IDPROM test
- APMU Mother Board - P/N:51740001 Rev:1012A S/N:
- APMU Relay Board - P/N:51740200 Rev:2060 S/N:
- APMU Rider Board - P/N:51740100 Rev:5200 S/N: 2
- APMU Rider Board - P/N:51740100 Rev:5200 S/N: 2
- APMU Rider Board - P/N:51740100 Rev:5200 S/N: 2
- APMU Rider Board - P/N:51740100 Rev:5200 S/N: 2
- APMU Rider Board - P/N:51740100 Rev:5200 S/N: 2
- APMU Rider Board - P/N:51740100 Rev:5200 S/N: 2
- APMU Rider Board - P/N:51740100 Rev:5200 S/N: 2
- APMU Rider Board - P/N:51740100 Rev:5200 S/N: 2
- Completed APMU IDPROM test
-
- Starting APMU Calibration on slot 5

- Completed APMU Calibration on slot 5

%JOB_END - ****PASSED**** APMU Calibration of slot 5 (S/N:4) at 11:43:48 AM

%JOB_START - Beginning ICUA Calibration test on slot 2 at 11:44:01 AM on 1/17/2020
Workbook Rev V7.60.40IP02 DC1116 IG-XL Version: 3.50.40IP02 DIB: P/N 51745600 S/N xxxxxxx Rev 0901A

%INFO - ----------
%INFO - System IP750_ (IP750EX)
%INFO - IG-XL 3.50.40IP02, Build: 04.13.11.20.00
%INFO - Maintenance 7.60.40IP02, Build: 04.18.11.02.09
%INFO - ----------
- Starting dib_test

- ICUA-2 P/N:51742601 Rev:738B S/N:4
- %INFO -- ADM on ICUA-2 Chan0 Slot2, ADM P/N:51740520 Rev:735C S/N:4
- %INFO -- ADM on ICUA-2 Chan1 Slot2, ADM P/N:51740520 Rev:735C S/N:4
- %INFO -- ADM on ICUA-2 Chan2 Slot2, ADM P/N:51740520 Rev:735C S/N:4
- %INFO -- ADM on ICUA-2 Chan3 Slot2, ADM P/N:51740520 Rev:735C S/N:4
- ICUA-2 Relay board P/N:51742800 Rev:515C S/N:4
- [ICUA Reference DAC Calibration]
- [ADM Range Calibration]
- - CDS Cal for AD9101
- - ICUA Chan 8 - (up to 1 min)
- - ICUA Chan 9 - (up to 1 min)
- - ICUA Chan 10 - (up to 1 min)
- - ICUA Chan 11 - (up to 1 min)
- [ADM DAC's Calibration]
- - ICUA Chan 8 -
- - ICUA Chan 9 -
- - ICUA Chan 10 -
- - ICUA Chan 11 -
- [Line Clamp Calibration]
- - ICUA Chan 8 -
- - ICUA Chan 8 -
- - ICUA Chan 9 -
- - ICUA Chan 9 -
- - ICUA Chan 10 -
- - ICUA Chan 10 -
- - ICUA Chan 11 -
- - ICUA Chan 11 -
- Complete ICUA Calibration 154.9 sec

%JOB_END - ****PASSED**** ICUA Calibration of slot 2 (S/N:4) at 11:46:36 AM

%JOB_START - Beginning AC Calibration at 11:46:48 AM on 1/17/2020 in High Accuracy Mode
Workbook Rev V7.60.40IP02 DC1116 IG-XL Version: 3.50.40IP02 DIB: P/N 51745600 S/N xxxxxxx Rev 0901A

%INFO - ----------
%INFO - System IP750_ (IP750EX)
%INFO - IG-XL 3.50.40IP02, Build: 04.13.11.20.00
%INFO - Maintenance 7.60.40IP02, Build: 04.18.11.02.09
%INFO - ----------
- Beginning Digital Channel Timing Calibration
- Building List of Digital Channels
- Checking CalDIB AC Continuity for all Digital Channels
- Calibrating Super Linear Interpolator (SLI)
- Measuring Cub Round Trip Delay
- Measuring RF Matrix Delay
- Calibrating Drive Edges
- Calibrating Receive Edges
- Calibrating Receive Window
- Calibrating HFMux
- Calibrating Mux Drive
- Calibrating Receive Mux

- Completed Digital Channel Timing Calibration

%JOB_END - ****PASSED**** AC Calibration at 11:49:40 AM

- Writing to System Calibration file - Begin (up to 5 minutes)
- Writing to System Calibration file – End

%JOB_START - Beginning ICUL1G Quick Check test on slot 16 at 12:39:25 PM on 1/17/2020
Workbook Rev V7.60.40IP02 DC1116 IG-XL Version: 3.50.40IP02 (P5) DIB: P/N 51745600 S/N Rev 0901A

%INFO - ----------
%INFO - System IP750_(IP750EX)
%INFO - IG-XL 3.50.40IP02 (P5), Build: 10.23.14.08.52
%INFO - Maintenance Not installed,
%INFO - ----------
- Started ICUL1G test on slot 16
- Started ICUL1G Board IDPROM Test...
- ICUL1G Mother Board - P/N:51746301 Rev:1114A S/N:
- ICUL1G Rider Board - P/N:51746400 Rev:1039A S/N:
- Completed ICUL1G Board IDPROM Test.

- Active Device Set: HighSpeed1.1.1

- Started ICUL1G Temperature Test...
- ICUL1G Board TempSensor0 Temperature: 30.5 degrees C
- ICUL1G Board TempSensor1 Temperature: 30.5 degrees C
- ICUL1G Board TempSensor2 Temperature: 28.0 degrees C
- ICUL1G Board TempSensor3 Temperature: 32.0 degrees C
- ICUL1G Board TempSensor4 Temperature: 23.0 degrees C
- Completed ICUL1G Temperature Test.

- Started ICUL1G POL Test...
- Completed ICUL1G POL Test.

- Started ICUL1G FPGA Rev. Test...
- Misc FPGA Rev : 0xE
- Misc FPGA Firmware Rev : 0x34
- Channel FPGA Rev : 0x22
- Infiniband FPGA Rev : 0xD
- Infiniband FPGA Firmware Rev : 0x20B
- Completed ICUL1G FPGA Rev Test.

- Started ICUL1G AT23 Temperature Test...
- Completed ICUL1G AT23 Temperature Test.

- Started ICUL1G FPGA Temperature Test...
- Completed ICUL1G FPGA Temperature Test.

- Started PG Register Test
- Completed PG Register Test

- Started PG LVM BIST
- Completed PG LVM BIST
- Started PG SVM Test
- Completed PG SVM Test
- Started FPGA Register Test
- Completed FPGA Register Test
- Started Misc FPGA Register Test.
- Completed Misc FPGA Register Test.
- Started FPGA Level Set Memory Test
- Completed FPGA Level Set Memory Test
- Started SDRAM Data Test
- Completed SDRAM Data Test

- Started ICUL1G ADC BIT Test...
- Completed ICUL1G ADC BIT Test.
- Started ICUL1G AT23 Comparator Test...
- Testing DUT Chan 48-51
- Testing DUT Chan 52-55
- Testing DUT Chan 56-59
- Testing DUT Chan 60-63
- Testing DUT Chan 64-67
- Testing DUT Chan 68-71
- Completed ICUL1G AT23 Comparator Test.
- Started InfiniBand State Test
- Check IDPConfig and RPC Ethernet Communication
- == Running with Image Processing PC(IMGPC0) ==
- Testing HCA Status Test
- Testing TCA Status Test
- Testing IB Status Test
- Completed InfiniBand State Test
- Started ICUL1G Frequency Counter Test
- Testing DUT Chan 48
- Testing DUT Chan 49
- Testing DUT Chan 50
- Testing DUT Chan 51
- Testing DUT Chan 52
- Testing DUT Chan 53
- Testing DUT Chan 54
- Testing DUT Chan 55
- Completed ICUL1G Frequency Counter Test
- Started ICUL1G Sync Code Test
- Testing Pin Group 0(Ch48/Ch56)
- Testing Pin Group 1(Ch49/Ch57)
- Testing Pin Group 2(Ch50/Ch58)
- Testing Pin Group 3(Ch51/Ch59)
- Testing Pin Group 4(Ch52/Ch60)
- Testing Pin Group 5(Ch53/Ch61)
- Testing Pin Group 6(Ch54/Ch62)
- Testing Pin Group 7(Ch55/Ch63)
- Completed ICUL1G Sync Code Test
- Started ICUL1G Serial Capture Test
- Test in 100M/DDR/NormalCapture/Serial1/1 Lane

- Test in 100M/DDR/NormalCapture/Serial1/2 Lane
- Test in 100M/DDR/NormalCapture/Serial1/4 Lane
- Test in 100M/DDR/NormalCapture/Serial1/16 Lane
- Test in 100M/DDR/NormalCapture/Serial2/1 Lane
- Test in 100M/DDR/NormalCapture/Serial2/2 Lane
- Test in 100M/DDR/NormalCapture/Serial2/3 Lane
- Test in 100M/DDR/NormalCapture/Serial2/4 Lane
- Test in 100M/DDR/NormalCapture/Serial3/16 Lane
- Test in 100M/DDR/RawCapture/Serial2/1 Lane
- Test in 100M/DDR/RawCapture/Serial2/2 Lane
- Test in 100M/DDR/RawCapture/Serial2/3 Lane
- Test in 100M/DDR/RawCapture/Serial2/4 Lane
- Test in 100M/DDR/RawCapture/Serial3/16 Lane
- Test in 100M/DDR/NormalCapture/Serial1/10 Lane
- Test in 100M/DDR/NormalCapture/Serial3/10 Lane
- Test in 100M/DDR/RawCapture/Serial3/10 Lane
- Completed ICUL1G Serial Capture Test
- Started ICUL1G Differential Polarity Test
- Completed ICUL1G Differential Polarity Test

- Completed ICUL1G test on slot 16

- Run time: 0.7 min

%JOB_END - ****PASSED**** ICUL1G Quick Check of slot 16 (S/N:) at 12:40:09 PM

%JOB_START - Beginning ICUL1G Calibration test on slot 16 at 12:40:30 PM on 1/17/2020
Workbook Rev V7.60.40IP02 DC1116 IG-XL Version: 3.50.40IP02 (P5) DIB: P/N 51745600 S/N Rev 0901A

%INFO - ----------
%INFO - System IP750_ (IP750EX)
%INFO - IG-XL 3.50.40IP02 (P5), Build: 10.23.14.08.52
%INFO - Maintenance Not installed,
%INFO - ----------
- ** Pre-Check before Calibration on slot 16 **
- Started ICUL1G Board IDPROM Test...
- ICUL1G Mother Board - P/N:51746301 Rev:1114A S/N:
- ICUL1G Rider Board - P/N:51746400 Rev:1039A S/N:
- Completed ICUL1G Board IDPROM Test.

- Active Device Set: HighSpeed1.1.1

- Started ICUL1G Temperature Test...
- ICUL1G Board TempSensor0 Temperature: 30.5 degrees C
- ICUL1G Board TempSensor1 Temperature: 30.5 degrees C
- ICUL1G Board TempSensor2 Temperature: 28.0 degrees C
- ICUL1G Board TempSensor3 Temperature: 32.0 degrees C
- ICUL1G Board TempSensor4 Temperature: 23.0 degrees C
- Completed ICUL1G Temperature Test.

- Started ICUL1G POL Test...

- Completed ICUL1G POL Test.

- Started ICUL1G FPGA Rev. Test...
- Misc FPGA Rev : 0xE
- Misc FPGA Firmware Rev : 0x34
- Channel FPGA Rev : 0x22
- Infiniband FPGA Rev : 0xD
- Infiniband FPGA Firmware Rev : 0x20B
- Completed ICUL1G FPGA Rev Test.

- Started ICUL1G AT23 Temperature Test...
- Completed ICUL1G AT23 Temperature Test.

- Started ICUL1G FPGA Temperature Test...
- Completed ICUL1G FPGA Temperature Test.

- ** Ended Pre-Check before Calibration **

- Started ICUL1G Calibration on slot 16
- Started CALBUS Cal
- Completed CALBUS Cal
-
- Started COMPDAC Cal
- Completed COMPDAC Cal
-
- Started PPMU FV Cal
- Completed PPMU FV Cal
-
- Started PPMU MV Cal
- Completed PPMU MV Cal
-
- Started PPMU IIOS Cal
- Completed PPMU IIOS Cal
-
- Started PPMU MI Cal
- Completed PPMU MI Cal
-
- Started PPMU FI Cal
- Completed PPMU FI Cal
-
- Started PE DRIVER Cal
- Completed PE DRIVER Cal
-
- Started PE IMPEDANCE Cal
- Completed PE IMPEDANCE Cal
-
- Started PE SE COMP Cal
- Completed PE SE COMP Cal
-
- Started PE DIFF COMP Cal
- Completed PE DIFF COMP Cal
-

- Started PPMU CURRENT-CLAMP Cal
- Completed PPMU CURRENT-CLAMP Cal
-
- Started PPMU VOLTAGE-CLAMP Cal
- Completed PPMU VOLTAGE-CLAMP Cal
-
- Started ICUL1G Walking Strobe Start Timing Calculation on slot 16
- Completed ICUL1G Walking Strobe Start Timing Calculation on slot 16

- Started ICUL1G Phase Adjustment SyncBit for Source and Capture on slot 16
- Completed ICUL1G Phase Adjustment SyncBit for Source and Capture on slot 16

- Started ICUL1G Phase Adjustment Test between REFCLK and Drive Sync Capture Enable Bit on
slot 16
- Completed ICUL1G Phase Adjustment Test between REFCLK and Drive Sync Capture Enable Bit
on slot 16

- Started ICUL1G Walking Strobe Start Timing Calculation on slot 16
- Completed ICUL1G Walking Strobe Start Timing Calculation on slot 16

- Started ICUL1G External Delay Calibration on slot 16
- Completed ICUL1G External Delay Calibration on slot 16

- Started ICUL1G IDelay Calibration on slot 16
- Completed ICUL1G IDelay Calibration on slot 16

- Started ICUL1G Internal Path Calibration on slot 16
- Completed ICUL1G Internal Path Calibration on slot 16

- Started ICUL1G Slave Drive Calibration on slot 16
- Completed ICUL1G Slave Drive Calibration on slot 16

- Started ICUL1G Slave Receive Calibration on slot 16
- Completed ICUL1G Slave Receive Calibration on slot 16

- Started ICUL1G AC CALTREE TDT Calibration on slot 16
- Completed ICUL1G AC CALTREE TDT Calibration on slot 16

- Started ICUL1G Drive Calibration on slot 16
- Completed ICUL1G Drive Calibration on slot 16

- Started ICUL1G Data-Clock Capture Calibration on slot 16
- Completed ICUL1G Data-Clock Capture Calibration on slot 16

- Completed ICUL1G Calibration on slot 16

- Run time: 7.7 min

%JOB_END - ****PASSED**** ICUL1G Calibration of slot 16 (S/N:) at 12:48:12 PM

- Writing to System Calibration file - Begin (up to 5 minutes)
- Writing to System Calibration file - End

%JOB_START - Beginning ICUL1G Module Check test on slot 16 at 12:48:39 PM on 1/17/2020
Workbook Rev V7.60.40IP02 DC1116 IG-XL Version: 3.50.40IP02 (P5) DIB:
P/N 51745600 S/N Rev 0901A

%INFO - ----------
%INFO - System IP750_ (IP750EX)
%INFO - IG-XL 3.50.40IP02 (P5), Build: 10.23.14.08.52
%INFO - Maintenance Not installed,
%INFO - ----------
- Started ICUL1G test on slot 16
- Started ICUL1G Board IDPROM Test...
- ICUL1G Mother Board - P/N:51746301 Rev:1114A S/N:
- ICUL1G Rider Board - P/N:51746400 Rev:1039A S/N:
- Completed ICUL1G Board IDPROM Test.

- Active Device Set: HighSpeed1.1.1

- Started ICUL1G Temperature Test...
- ICUL1G Board TempSensor0 Temperature: 30.5 degrees C
- ICUL1G Board TempSensor1 Temperature: 31.0 degrees C
- ICUL1G Board TempSensor2 Temperature: 28.5 degrees C
- ICUL1G Board TempSensor3 Temperature: 32.0 degrees C
- ICUL1G Board TempSensor4 Temperature: 23.5 degrees C
- Completed ICUL1G Temperature Test.

- Started ICUL1G POL Test...
- Completed ICUL1G POL Test.

- Started ICUL1G FPGA Rev. Test...
- Misc FPGA Rev : 0xE
- Misc FPGA Firmware Rev : 0x34
- Channel FPGA Rev : 0x22
- Infiniband FPGA Rev : 0xD
- Infiniband FPGA Firmware Rev : 0x20B
- Completed ICUL1G FPGA Rev Test.

- Started ICUL1G AT23 Temperature Test...
- Completed ICUL1G AT23 Temperature Test.

- Started ICUL1G FPGA Temperature Test...
- Completed ICUL1G FPGA Temperature Test.

- Started PG Register Test
- Completed PG Register Test
- Started PG LVM BIST
- takes about 1 min...
- Completed PG LVM BIST
- Started PG SVM Test
- Completed PG SVM Test
- Started FPGA Register Test

- Completed FPGA Register Test
- Started Misc FPGA Register Test.
- Completed Misc FPGA Register Test.
- Started FPGA Level Set Memory Test
- Completed FPGA Level Set Memory Test
- Started SDRAM Data Test
- takes about 10 sec...
- Completed SDRAM Data Test

- Started ICUL1G ADC BIT Test...
- Completed ICUL1G ADC BIT Test.
- Started ICUL1G AT23 Comparator Test...
- Testing DUT Chan 48-51
- Testing DUT Chan 52-55
- Testing DUT Chan 56-59
- Testing DUT Chan 60-63
- Testing DUT Chan 64-67
- Testing DUT Chan 68-71
- Completed ICUL1G AT23 Comparator Test.

- Started ICUL1G DUT Relay Test...
- Completed ICUL1G DUT Relay Test.
- Started PPMU FV Test
- Testing DUT Chan 48-51
- Testing DUT Chan 52-55
- Testing DUT Chan 56-59
- Testing DUT Chan 60-63
- Testing DUT Chan 64-67
- Testing DUT Chan 68-71
- Completed PPMU FV Test
- Started PPMU MV Test
- Testing DUT Chan 48-51
- Testing DUT Chan 52-55
- Testing DUT Chan 56-59
- Testing DUT Chan 60-63
- Testing DUT Chan 64-67
- Testing DUT Chan 68-71
- Completed PPMU MV Test
- Started PPMU FI Test
- Testing DUT Chan 48-51
- Testing DUT Chan 52-55
- Testing DUT Chan 56-59
- Testing DUT Chan 60-63
- Testing DUT Chan 64-67
- Testing DUT Chan 68-71
- Completed PPMU FI Test
- Started PPMU MI Test
- Testing DUT Chan 48-51
- Testing DUT Chan 52-55
- Testing DUT Chan 56-59
- Testing DUT Chan 60-63
- Testing DUT Chan 64-67

- Testing DUT Chan 68-71
- Completed PPMU MI Test
- Started PPMU V Clamp Test
- Testing DUT Chan 48-51
- Testing DUT Chan 52-55
- Testing DUT Chan 56-59
- Testing DUT Chan 60-63
- Testing DUT Chan 64-67
- Testing DUT Chan 68-71
- Completed PPMU V Clamp Test
- Started ICUL1G DGS Test...
- Completed ICUL1G DGS Test.

- Started InfiniBand State Test
- Check IDPConfig and RPC Ethernet Communication
- == Running with Image Processing PC(IMGPC0) ==
- Testing HCA Status Test
- Testing TCA Status Test
- Testing IB Status Test
- Completed InfiniBand State Test
- Started ICUL1G State Bus Test
- Check Capture_Enable/Disable U-code
- Testing NORMAL
- Testing EXTENDED
- Testing QUAD
- Check FrequencyCounter_Start U-code
- Testing NORMAL
- Testing EXTENDED
- Testing QUAD
- Completed ICUL1G State Bus Test
- Started XFER Test
- Testing Pin Group 0(Ch48/Ch56)
- Testing Pin Group 1(Ch49/Ch57)
- Testing Pin Group 2(Ch50/Ch58)
- Testing Pin Group 3(Ch51/Ch59)
- Testing Pin Group 4(Ch52/Ch60)
- Testing Pin Group 5(Ch53/Ch61)
- Testing Pin Group 6(Ch54/Ch62)
- Testing Pin Group 7(Ch55/Ch63)
- Completed XFER Test
- Started ICUL1G Frequency Counter Test
- Testing DUT Chan 48
- Testing DUT Chan 49
- Testing DUT Chan 50
- Testing DUT Chan 51
- Testing DUT Chan 52
- Testing DUT Chan 53
- Testing DUT Chan 54
- Testing DUT Chan 55
- Completed ICUL1G Frequency Counter Test
- Started ICUL1G Pixel/Line Size Test
- Testing Pin Group 0(Ch48/Ch56)

- Testing Pin Group 1(Ch49/Ch57)
- Testing Pin Group 2(Ch50/Ch58)
- Testing Pin Group 3(Ch51/Ch59)
- Testing Pin Group 4(Ch52/Ch60)
- Testing Pin Group 5(Ch53/Ch61)
- Testing Pin Group 6(Ch54/Ch62)
- Testing Pin Group 7(Ch55/Ch63)
- Completed ICUL1G Pixel/Line Size Test
- Started ICUL1G Frame Count Test
- Testing Pin Group 0(Ch48/Ch56)
- Testing Pin Group 1(Ch49/Ch57)
- Testing Pin Group 2(Ch50/Ch58)
- Testing Pin Group 3(Ch51/Ch59)
- Testing Pin Group 4(Ch52/Ch60)
- Testing Pin Group 5(Ch53/Ch61)
- Testing Pin Group 6(Ch54/Ch62)
- Testing Pin Group 7(Ch55/Ch63)
- Completed ICUL1G Frame Count Test
- Started ICUL1G Line HoldOff Test
- Testing Pin Group 0(Ch48/Ch56)
- Testing Pin Group 1(Ch49/Ch57)
- Testing Pin Group 2(Ch50/Ch58)
- Testing Pin Group 3(Ch51/Ch59)
- Testing Pin Group 4(Ch52/Ch60)
- Testing Pin Group 5(Ch53/Ch61)
- Testing Pin Group 6(Ch54/Ch62)
- Testing Pin Group 7(Ch55/Ch63)
- Completed ICUL1G Line HoldOff Test
- Started ICUL1G Frame HoldOff Test
- Testing Pin Group 0(Ch48/Ch56)
- Testing Pin Group 1(Ch49/Ch57)
- Testing Pin Group 2(Ch50/Ch58)
- Testing Pin Group 3(Ch51/Ch59)
- Testing Pin Group 4(Ch52/Ch60)
- Testing Pin Group 5(Ch53/Ch61)
- Testing Pin Group 6(Ch54/Ch62)
- Testing Pin Group 7(Ch55/Ch63)
- Completed ICUL1G Frame HoldOff Test
- Started ICUL1G Sync HoldOff Test
- Testing Pin Group 0(Ch48/Ch56)
- Testing Pin Group 1(Ch49/Ch57)
- Testing Pin Group 2(Ch50/Ch58)
- Testing Pin Group 3(Ch51/Ch59)
- Testing Pin Group 4(Ch52/Ch60)
- Testing Pin Group 5(Ch53/Ch61)
- Testing Pin Group 6(Ch54/Ch62)
- Testing Pin Group 7(Ch55/Ch63)
- Completed ICUL1G Sync HoldOff Test
- Started ICUL1G Sync Code Test
- Testing Pin Group 0(Ch48/Ch56)
- Testing Pin Group 1(Ch49/Ch57)
- Testing Pin Group 2(Ch50/Ch58)

- Testing Pin Group 3(Ch51/Ch59)
- Testing Pin Group 4(Ch52/Ch60)
- Testing Pin Group 5(Ch53/Ch61)
- Testing Pin Group 6(Ch54/Ch62)
- Testing Pin Group 7(Ch55/Ch63)
- Completed ICUL1G Sync Code Test
- Started ICUL1G Pixel Clipping Alarm Test
- Testing Pin Group 0(Ch48/Ch56)
- Testing Pin Group 1(Ch49/Ch57)
- Testing Pin Group 2(Ch50/Ch58)
- Testing Pin Group 3(Ch51/Ch59)
- Testing Pin Group 4(Ch52/Ch60)
- Testing Pin Group 5(Ch53/Ch61)
- Testing Pin Group 6(Ch54/Ch62)
- Testing Pin Group 7(Ch55/Ch63)
- Completed ICUL1G Pixel Clipping Alarm Test
- Started ICUL1G Line Clipping Alarm Test
- Testing Pin Group 0(Ch48/Ch56)
- Testing Pin Group 1(Ch49/Ch57)
- Testing Pin Group 2(Ch50/Ch58)
- Testing Pin Group 3(Ch51/Ch59)
- Testing Pin Group 4(Ch52/Ch60)
- Testing Pin Group 5(Ch53/Ch61)
- Testing Pin Group 6(Ch54/Ch62)
- Testing Pin Group 7(Ch55/Ch63)
- Completed ICUL1G Line Clipping Alarm Test
- Started ICUL1G Frequency Counter Alarm Test
- Testing DUT Chan 48
- Testing DUT Chan 49
- Testing DUT Chan 50
- Testing DUT Chan 51
- Testing DUT Chan 52
- Testing DUT Chan 53
- Testing DUT Chan 54
- Testing DUT Chan 55
- Completed ICUL1G Frequency Counter Alarm Test
- Started ICUL1G VSync Interval Alarm Test
- Testing Pin Group 0(Ch48/Ch56)
- Testing Pin Group 1(Ch49/Ch57)
- Testing Pin Group 2(Ch50/Ch58)
- Testing Pin Group 3(Ch51/Ch59)
- Testing Pin Group 4(Ch52/Ch60)
- Testing Pin Group 5(Ch53/Ch61)
- Testing Pin Group 6(Ch54/Ch62)
- Testing Pin Group 7(Ch55/Ch63)
- Completed ICUL1G VSync Interval Alarm Test
- Started ICUL1G Serial Capture Test
- Test in 100M/DDR/NormalCapture/Serial1/1 Lane
- Test in 300M/DDR/NormalCapture/Serial1/1 Lane
- Test in 100M/DDR/NormalCapture/Serial1/2 Lane
- Test in 300M/DDR/NormalCapture/Serial1/2 Lane
- Test in 100M/DDR/NormalCapture/Serial1/4 Lane

- Test in 300M/DDR/NormalCapture/Serial1/4 Lane
- Test in 100M/DDR/NormalCapture/Serial1/16 Lane
- Test in 300M/DDR/NormalCapture/Serial1/16 Lane
- Test in 100M/DDR/NormalCapture/Serial2/1 Lane
- Test in 300M/DDR/NormalCapture/Serial2/1 Lane
- Test in 100M/DDR/NormalCapture/Serial2/2 Lane
- Test in 300M/DDR/NormalCapture/Serial2/2 Lane
- Test in 100M/DDR/NormalCapture/Serial2/3 Lane
- Test in 300M/DDR/NormalCapture/Serial2/3 Lane
- Test in 100M/DDR/NormalCapture/Serial2/4 Lane
- Test in 300M/DDR/NormalCapture/Serial2/4 Lane
- Test in 100M/DDR/NormalCapture/Serial3/16 Lane
- Test in 300M/DDR/NormalCapture/Serial3/16 Lane
- Test in 100M/DDR/RawCapture/Serial2/1 Lane
- Test in 300M/DDR/RawCapture/Serial2/1 Lane
- Test in 100M/DDR/RawCapture/Serial2/2 Lane
- Test in 300M/DDR/RawCapture/Serial2/2 Lane
- Test in 100M/DDR/RawCapture/Serial2/3 Lane
- Test in 300M/DDR/RawCapture/Serial2/3 Lane
- Test in 100M/DDR/RawCapture/Serial2/4 Lane
- Test in 300M/DDR/RawCapture/Serial2/4 Lane
- Test in 100M/DDR/RawCapture/Serial3/16 Lane
- Test in 300M/DDR/RawCapture/Serial3/16 Lane
- Test in 100M/DDR/NormalCapture/Serial1/10 Lane
- Test in 300M/DDR/NormalCapture/Serial1/10 Lane
- Test in 100M/DDR/NormalCapture/Serial3/10 Lane
- Test in 300M/DDR/NormalCapture/Serial3/10 Lane
- Test in 100M/DDR/RawCapture/Serial3/10 Lane
- Test in 300M/DDR/RawCapture/Serial3/10 Lane
- Completed ICUL1G Serial Capture Test
- Started ICUL1G Differential Polarity Test
- Completed ICUL1G Differential Polarity Test
- Completed ICUL1G test on slot 16

- Run time: 8.5 min

%JOB_END - ****PASSED**** ICUL1G Module Check of slot 16 (S/N:) at 12:57:11 PM

%JOB_START - Beginning ICUL1G Performance Verification test on slot 16 at 12:57:34 PM on 1/17/2020
Workbook Rev V7.60.40IP02 DC1116 IG-XL Version: 3.50.40IP02 (P5) DIB: P/N 51745600 S/N Rev 0901A

%INFO - ----------
%INFO - System IP750_ (IP750EX)
%INFO - IG-XL 3.50.40IP02 (P5), Build: 10.23.14.08.52
%INFO - Maintenance Not installed,
%INFO - ----------
- Started ICUL1G test on slot 16
- Started ICUL1G Board IDPROM Test...
- ICUL1G Mother Board - P/N:51746301 Rev:1114A S/N:
- ICUL1G Rider Board - P/N:51746400 Rev:1039A S/N:

- Completed ICUL1G Board IDPROM Test.

- Active Device Set: HighSpeed1.1.1

- Started ICUL1G Temperature Test...
- ICUL1G Board TempSensor0 Temperature: 31.0 degrees C
- ICUL1G Board TempSensor1 Temperature: 31.0 degrees C
- ICUL1G Board TempSensor2 Temperature: 28.5 degrees C
- ICUL1G Board TempSensor3 Temperature: 32.0 degrees C
- ICUL1G Board TempSensor4 Temperature: 23.5 degrees C
- Completed ICUL1G Temperature Test.

- Started ICUL1G POL Test...
- Completed ICUL1G POL Test.

- Started ICUL1G FPGA Rev. Test...
- Misc FPGA Rev : 0xE
- Misc FPGA Firmware Rev : 0x34
- Channel FPGA Rev : 0x22
- Infiniband FPGA Rev : 0xD
- Infiniband FPGA Firmware Rev : 0x20B
- Completed ICUL1G FPGA Rev Test.

- Started ICUL1G AT23 Temperature Test...
- Completed ICUL1G AT23 Temperature Test.

- Started ICUL1G FPGA Temperature Test...
- Completed ICUL1G FPGA Temperature Test.

- Started PPMU FV Performance Test
- Testing DUT Chan 48-51
- Testing DUT Chan 52-55
- Testing DUT Chan 56-59
- Testing DUT Chan 60-63
- Testing DUT Chan 64-67
- Testing DUT Chan 68-71
- Completed PPMU FV Performance Test
- Started PPMU MV Performance Test
- Testing DUT Chan 48-51
- Testing DUT Chan 52-55
- Testing DUT Chan 56-59
- Testing DUT Chan 60-63
- Testing DUT Chan 64-67
- Testing DUT Chan 68-71
- Completed PPMU MV Performance Test
- Started PPMU FI Performance Test
- Testing DUT Chan 48-51
- Testing DUT Chan 52-55
- Testing DUT Chan 56-59
- Testing DUT Chan 60-63
- Testing DUT Chan 64-67
- Testing DUT Chan 68-71

- Completed PPMU FI Performance Test
- Started PPMU MI Performance Test
- Testing DUT Chan 48-51
- Testing DUT Chan 52-55
- Testing DUT Chan 56-59
- Testing DUT Chan 60-63
- Testing DUT Chan 64-67
- Testing DUT Chan 68-71
- Completed PPMU MI Performance Test
- Started PPMU V Clamp Performance Test
- Testing DUT Chan 48-51
- Testing DUT Chan 52-55
- Testing DUT Chan 56-59
- Testing DUT Chan 60-63
- Testing DUT Chan 64-67
- Testing DUT Chan 68-71
- Completed PPMU V Clamp Performance Test
- Started InfiniBand State Test
- Check IDPConfig and RPC Ethernet Communication
- == Running with Image Processing PC(IMGPC0) ==
- Testing HCA Status Test
- Testing TCA Status Test
- Testing IB Status Test
- Completed InfiniBand State Test
- Started ICUL1G Serial Capture Test
- Test in 100M/DDR/NormalCapture/Serial1/1 Lane
- Test in 300M/DDR/NormalCapture/Serial1/1 Lane
- Test in 100M/DDR/NormalCapture/Serial1/2 Lane
- Test in 300M/DDR/NormalCapture/Serial1/2 Lane
- Test in 100M/DDR/NormalCapture/Serial1/4 Lane
- Test in 300M/DDR/NormalCapture/Serial1/4 Lane
- Test in 100M/DDR/NormalCapture/Serial1/16 Lane
- Test in 300M/DDR/NormalCapture/Serial1/16 Lane
- Test in 100M/DDR/NormalCapture/Serial2/1 Lane
- Test in 300M/DDR/NormalCapture/Serial2/1 Lane
- Test in 100M/DDR/NormalCapture/Serial2/2 Lane
- Test in 300M/DDR/NormalCapture/Serial2/2 Lane
- Test in 100M/DDR/NormalCapture/Serial2/3 Lane
- Test in 300M/DDR/NormalCapture/Serial2/3 Lane
- Test in 100M/DDR/NormalCapture/Serial2/4 Lane
- Test in 300M/DDR/NormalCapture/Serial2/4 Lane
- Test in 100M/DDR/NormalCapture/Serial3/16 Lane
- Test in 300M/DDR/NormalCapture/Serial3/16 Lane
- Test in 100M/DDR/RawCapture/Serial2/1 Lane
- Test in 300M/DDR/RawCapture/Serial2/1 Lane
- Test in 100M/DDR/RawCapture/Serial2/2 Lane
- Test in 300M/DDR/RawCapture/Serial2/2 Lane
- Test in 100M/DDR/RawCapture/Serial2/3 Lane
- Test in 300M/DDR/RawCapture/Serial2/3 Lane
- Test in 100M/DDR/RawCapture/Serial2/4 Lane
- Test in 300M/DDR/RawCapture/Serial2/4 Lane
- Test in 100M/DDR/RawCapture/Serial3/16 Lane

- Test in 300M/DDR/RawCapture/Serial3/16 Lane
- Test in 100M/DDR/NormalCapture/Serial1/10 Lane
- Test in 300M/DDR/NormalCapture/Serial1/10 Lane
- Test in 100M/DDR/NormalCapture/Serial3/10 Lane
- Test in 300M/DDR/NormalCapture/Serial3/10 Lane
- Test in 100M/DDR/RawCapture/Serial3/10 Lane
- Test in 300M/DDR/RawCapture/Serial3/10 Lane
- Completed ICUL1G Serial Capture Test
- Completed ICUL1G test on slot 16

- Run time: 4.4 min

%JOB_END - ****PASSED**** ICUL1G Performance Verification of slot 16 (S/N:) at 1:01:55 PM

%JOB_START - Beginning systemwide tests at 11:27:39 AM on 1/17/2020
Workbook Rev V7.60.40IP02 DC1116 IG-XL Version: 3.50.40IP02 DIB: P/N 51745600 S/N xxxxxxx Rev 0901A

%INFO - ----------
%INFO - System IP750 (IP750EX)
%INFO - IG-XL 3.50.40IP02, Build: 04.13.11.20.00
%INFO - Maintenance 7.60.40IP02, Build: 04.18.11.02.09
%INFO - ----------
- Systemwide functionality and continuity to slot 0
- Systemwide functionality and continuity to slot 1
- Starting BackPlane Fail Bus test
- Completed BackPlane Fail Bus test
- Completed Extra

%JOB_END - ****PASSED**** Systemwide tests at 11:27:41 AM

%JOB_START - Beginning CUB Module Check test on slot 18 at 11:27:52 AM on 1/17/2020
Workbook Rev V7.60.40IP02 DC1116 IG-XL Version: 3.50.40IP02 DIB: P/N 51745600 S/N xxxxxxx Rev 0901A

%INFO - ----------
%INFO - System IP750_(IP750EX)
%INFO - IG-XL 3.50.40IP02, Build: 04.13.11.20.00
%INFO - Maintenance 7.60.40IP02, Build: 04.18.11.02.09
%INFO - ----------
- Testing CalCUB and CalDIB Leakage
- Completed Cal Dib Leakage Test
- Testing CalCUB Voltage Sources on CalDIB
- Beginning Cal DIB RawV Test on Slot18
- Completed Cal DIB RawV Test on Slot 18
- Beginning Cal Dib to BPMU Test on Slot 0
- Completed Cal Dib to BPMU Test on Slot 0
- Beginning Cal Dib to EXTERN Test on Slot 0
- Completed Cal Dib to EXTERN Test on Slot 0
- Testing CalDIB Utility Bit Relays using Channel Board Utility Bits for Slot 0

- Completed Cal Dib to UTIL Test on Slot 0
- Beginning Cal Dib RF Tree & Pogo Test

- Beginning Cal Dib to BPMU Test on Slot 1
- Completed Cal Dib to BPMU Test on Slot 1
- Beginning Cal Dib to EXTERN Test on Slot 1
- Completed Cal Dib to EXTERN Test on Slot 1
- Testing CalDIB Utility Bit Relays using Channel Board Utility Bits for Slot 1
- Completed Cal Dib to UTIL Test on Slot 1
- Beginning Cal Dib RF Tree & Pogo Test

- Beginning Cal DIB to DPS_FSG Test on Slot 22
- Completed Cal DIB to DPS_FSG Test on Slot 22
- Testing Device Ground Sense on CalDIB
- Completed DGS Test
- ****Completed CalDib Test****
- Start Compare Level Vol test
- Completed Compare Level Vol test
- Start Compare Level Voh test
- Completed Compare Level Voh test
- Start Drive_Level_test VIL
- Completed Drive_Level_test VIL
- Start Drive_Level_test VIH
- Completed Drive_Level_test VIH
- Beginning CalCub_Measure_Current using Bpmu in Slot 0
- Completed CalCub_Measure_Current

%JOB_END - ****PASSED**** CUB Module Check of slot 18 (S/N:XXXXXXX) at 11:28:20 AM

%JOB_START - Beginning CUB Calibration test on slot 18 at 11:29:14 AM on 1/17/2020
Workbook Rev V7.60.40IP02 DC1116 IG-XL Version: 3.50.40IP02 DIB: P/N 51745600 S/N xxxxxxx Rev 0901A

%INFO - ----------
%INFO - System IP750 (IP750EX)
%INFO - IG-XL 3.50.40IP02, Build: 04.13.11.20.00
%INFO - Maintenance 7.60.40IP02, Build: 04.18.11.02.09
%INFO - ----------
- Starting Channel Drive Levels: Vih Vil
- Starting Channel Compare Levels: Voh Vol
- Finished Channel Calibration

%JOB_END - ****PASSED**** CUB Calibration of slot 18 (S/N:XXXXXXXX) at 11:29:14 AM

%JOB_START - Beginning Channel_Board_DIB Calibration test on slot(s) 0,1 at 11:29:27 AM on 1/17/2020
Workbook Rev V7.60.40IP02 DC1116 IG-XL Version: 3.50.40IP02 DIB: P/N 51745600 S/N xxxxxxx Rev 0901A

%INFO - ----------

%INFO - System IP750(IP750EX)
%INFO - IG-XL 3.50.40IP02, Build: 04.13.11.20.00
%INFO - Maintenance 7.60.40IP02, Build: 04.18.11.02.09
%INFO - ----------
- Starting DC Calibration on slot 0
- Systemwide functionality and continuity to slot 0
- Starting dib_test
- Temperature at PE Ch00 is 38 deg C
- Temperature at PE Ch60 is 37 deg C
- Temperature at TG Ch60 is 26 deg C
- Temperature at TG Ch00 is 48 deg C
- Starting BPMU Force Voltage
- Starting Bpmu Clamp Voltage
- Starting Bpmu Measure Voltage
- Starting Bpmu Measure Current
- Starting Bpmu Force current
- Starting Bpmu Limit current
- Starting Channel Drive Levels: Vih Vil
- Starting Channel Drive Levels: VT50ohm
- Starting Channel Compare Levels: Voh Vol
- Starting Channel Clamps: Vch Vcl
- Starting Channel Loads: Ioh Iol
- Starting Channel Load Threshold: Vt
- Starting HV Channel Drive Levels
- Starting HV Channel Drive Current
- Starting FHV Channel Drive Levels
- Ppmu Mi Warmup 11:31:34 AM
- Ppmu Mi Warmup 11:31:34 AM
- Starting Ppmu Force Voltage
- Starting Ppmu Measure Voltage
- Starting Ppmu Force Current Ppmu Force 200ua
- Starting Ppmu Force Current Ppmu Force 2ma
- Starting Ppmu Force Current Ppmu Force 50ma
- Starting Ppmu Force Current Ppmu Force 20ua
- Starting Ppmu Measure 2ma
- Continuing Ppmu Measure Current chan 15
- Continuing Ppmu Measure Current chan 31
- Continuing Ppmu Measure Current chan 47
- Continuing Ppmu Measure Current chan 63
- Starting Ppmu Measure 200ua
- Continuing Ppmu Measure Current chan 15
- Continuing Ppmu Measure Current chan 31
- Continuing Ppmu Measure Current chan 47
- Continuing Ppmu Measure Current chan 63
- Starting Ppmu Measure 20ua
- Continuing Ppmu Measure Current chan 15
- Continuing Ppmu Measure Current chan 31
- Continuing Ppmu Measure Current chan 47
- Continuing Ppmu Measure Current chan 63
- Starting Ppmu Measure 2ua
- Continuing Ppmu Measure Current chan 15
- Continuing Ppmu Measure Current chan 31

- Continuing Ppmu Measure Current chan 47
- Continuing Ppmu Measure Current chan 63
- Starting Ppmu Measure 50ma
- Continuing Ppmu Measure Current chan 15
- Continuing Ppmu Measure Current chan 31
- Continuing Ppmu Measure Current chan 47
- Continuing Ppmu Measure Current chan 63
- Finished Channel Calibration
- Finished DC Calibration on slot 0
- Starting DC Calibration on slot 1
- Systemwide functionality and continuity to slot 1
- Starting dib_test
- Temperature at PE Ch00 is 36 deg C
- Temperature at PE Ch60 is 36 deg C
- Temperature at TG Ch60 is 25 deg C
- Temperature at TG Ch00 is 45 deg C
- Starting BPMU Force Voltage
- Starting Bpmu Clamp Voltage
- Starting Bpmu Measure Voltage
- Starting Bpmu Measure Current
- Starting Bpmu Force current
- Starting Bpmu Limit current
- Starting Channel Drive Levels: Vih Vil
- Starting Channel Drive Levels: VT50ohm
- Starting Channel Compare Levels: Voh Vol
- Starting Channel Clamps: Vch Vcl
- Starting Channel Loads: Ioh Iol
- Starting Channel Load Threshold: Vt
- Starting HV Channel Drive Levels
- Starting HV Channel Drive Current
- Starting FHV Channel Drive Levels
- Ppmu Mi Warmup 11:37:11 AM
- Ppmu Mi Warmup 11:37:11 AM
- Starting Ppmu Force Voltage
- Starting Ppmu Measure Voltage
- Starting Ppmu Force Current Ppmu Force 200ua
- Starting Ppmu Force Current Ppmu Force 2ma
- Starting Ppmu Force Current Ppmu Force 50ma
- Starting Ppmu Force Current Ppmu Force 20ua
- Starting Ppmu Measure 2ma
- Continuing Ppmu Measure Current chan 79
- Continuing Ppmu Measure Current chan 95
- Continuing Ppmu Measure Current chan 111
- Continuing Ppmu Measure Current chan 127
- Starting Ppmu Measure 200ua
- Continuing Ppmu Measure Current chan 79
- Continuing Ppmu Measure Current chan 95
- Continuing Ppmu Measure Current chan 111
- Continuing Ppmu Measure Current chan 127
- Starting Ppmu Measure 20ua
- Continuing Ppmu Measure Current chan 79
- Continuing Ppmu Measure Current chan 95

- Continuing Ppmu Measure Current chan 111
- Continuing Ppmu Measure Current chan 127
- Starting Ppmu Measure 2ua
- Continuing Ppmu Measure Current chan 79
- Continuing Ppmu Measure Current chan 95
- Continuing Ppmu Measure Current chan 111
- Continuing Ppmu Measure Current chan 127
- Starting Ppmu Measure 50ma
- Continuing Ppmu Measure Current chan 79
- Continuing Ppmu Measure Current chan 95
- Continuing Ppmu Measure Current chan 111
- Continuing Ppmu Measure Current chan 127
- Finished Channel Calibration
- Finished DC Calibration on slot 1

%JOB_END - ****PASSED**** Channel_Board_DIB Calibration of slot(s) 0, 1 at 11:40:41 AM
- PASS slot 0 (S/N XXXXXXX)
- PASS slot 1 (S/N XXXXXXX)

%JOB_START - Beginning DPS_DIB Calibration test on slot 22 at 11:40:54 AM on 1/17/2020
Workbook Rev V7.60.40IP02 DC1116 IG-XL Version: 3.50.40IP02 DIB: P/N 51745600 S/N xxxxxxx Rev 0901A

%INFO - ----------
%INFO - System IP750_E (IP750EX)
%INFO - IG-XL 3.50.40IP02, Build: 04.13.11.20.00
%INFO - Maintenance 7.60.40IP02, Build: 04.18.11.02.09
%INFO - ----------
- Starting DPS Calibration on slot 22

- Calibrating DPS Voltage on slot 22
- Calibrating DPS Current Limit on slot 22
- Calibrating DPS Current Measure (50uA Range) on slot 22
- Calibrating DPS Current Measure (500uA Range) on slot 22
- Calibrating DPS Current Measure (10mA Range) on slot 22
- Calibrating DPS Current Measure (100mA Range) on slot 22
- Calibrating DPS Current Measure (1A Range) on slot 22

- Finished DPS Calibration on slot 22

%JOB_END - ****PASSED**** DPS_DIB Calibration of slot 22 (S/N:XXXXXXXX) at 11:41:17 AM

%JOB_START - Beginning APMU Calibration test on slot 5 at 11:41:30 AM on 1/17/2020
Workbook Rev V7.60.40IP02 DC1116 IG-XL Version: 3.50.40IP02 DIB: P/N 51745600 S/N xxxxxxx Rev 0901A

%INFO - ----------
%INFO - System IP750_E (IP750EX)
%INFO - IG-XL 3.50.40IP02, Build: 04.13.11.20.00
%INFO - Maintenance 7.60.40IP02, Build: 04.18.11.02.09

%INFO - ----------
- Starting APMU IDPROM test
- APMU Mother Board - P/N:51740001 Rev:1012A S/N: xxxxxxxx
- APMU Relay Board - P/N:51740200 Rev:2060 S/N:
- APMU Rider Board - P/N:51740100 Rev:5200 S/N:
- APMU Rider Board - P/N:51740100 Rev:5200 S/N:
- APMU Rider Board - P/N:51740100 Rev:5200 S/N:
- APMU Rider Board - P/N:51740100 Rev:5200 S/N:
- APMU Rider Board - P/N:51740100 Rev:5200 S/N:
- APMU Rider Board - P/N:51740100 Rev:5200 S/N:
- APMU Rider Board - P/N:51740100 Rev:5200 S/N:
- Completed APMU IDPROM test
-
- Starting APMU Calibration on slot 5

- Completed APMU Calibration on slot 5

%JOB_END - ****PASSED**** APMU Calibration of slot 5 (S/N:xxxxxxxx) at 11:43:48 AM

%JOB_START - Beginning ICUA Calibration test on slot 2 at 11:44:01 AM on 1/17/2020
Workbook Rev V7.60.40IP02 DC1116 IG-XL Version: 3.50.40IP02 DIB: P/N 51745600 S/N xxxxxxx Rev 0901A

%INFO - ----------
%INFO - System IP750_E (IP750EX)
%INFO - IG-XL 3.50.40IP02, Build: 04.13.11.20.00
%INFO - Maintenance 7.60.40IP02, Build: 04.18.11.02.09
%INFO - ----------
- Starting dib_test
- ICUA-2 P/N:51742601 Rev:738B S/N:
- %INFO -- ADM on ICUA-2 Chan0 Slot2, ADM P/N:51740520 Rev:735C S/N:
- %INFO -- ADM on ICUA-2 Chan1 Slot2, ADM P/N:51740520 Rev:735C S/N:
- %INFO -- ADM on ICUA-2 Chan2 Slot2, ADM P/N:51740520 Rev:735C S/N:
- %INFO -- ADM on ICUA-2 Chan3 Slot2, ADM P/N:51740520 Rev:735C S/N:
- ICUA-2 Relay board P/N:51742800 Rev:515C S/N:
- [ICUA Reference DAC Calibration]
- [ADM Range Calibration]
- - CDS Cal for AD9101
- - ICUA Chan 8 - (up to 1 min)
- - ICUA Chan 9 - (up to 1 min)
- - ICUA Chan 10 - (up to 1 min)
- - ICUA Chan 11 - (up to 1 min)
- [ADM DAC's Calibration]
- - ICUA Chan 8 -
- - ICUA Chan 9 -
- - ICUA Chan 10 -
- - ICUA Chan 11 -
- [Line Clamp Calibration]
- - ICUA Chan 8 -

- - ICUA Chan 8 -
- - ICUA Chan 9 -
- - ICUA Chan 9 -
- - ICUA Chan 10 -
- - ICUA Chan 10 -
- - ICUA Chan 11 -
- - ICUA Chan 11 -
- Complete ICUA Calibration 154.9 sec

%JOB_END - ****PASSED**** ICUA Calibration of slot 2 (S/N:) at 11:46:36 AM

%JOB_START - Beginning AC Calibration at 11:46:48 AM on 1/17/2020 in High Accuracy Mode
Workbook Rev V7.60.40IP02 DC1116 IG-XL Version: 3.50.40IP02 DIB: P/N 51745600 S/N xxxxxxx Rev 0901A

%INFO - ----------
%INFO - System IP750_E (IP750EX)
%INFO - IG-XL 3.50.40IP02, Build: 04.13.11.20.00
%INFO - Maintenance 7.60.40IP02, Build: 04.18.11.02.09
%INFO - ----------
- Beginning Digital Channel Timing Calibration
- Building List of Digital Channels
- Checking CalDIB AC Continuity for all Digital Channels
- Calibrating Super Linear Interpolator (SLI)
- Measuring Cub Round Trip Delay
- Measuring RF Matrix Delay
- Calibrating Drive Edges
- Calibrating Receive Edges
- Calibrating Receive Window
- Calibrating HFMux
- Calibrating Mux Drive
- Calibrating Receive Mux
- Completed Digital Channel Timing Calibration

%JOB_END - ****PASSED**** AC Calibration at 11:49:40 AM

- Writing to System Calibration file - Begin (up to 5 minutes)
- Writing to System Calibration file - End
%JOB_START - Beginning systemwide tests at 11:51:24 AM on 1/17/2020
Workbook Rev V7.60.40IP02 DC1116 IG-XL Version: 3.50.40IP02 DIB: P/N 51745600 S/N xxxxxxx Rev 0901A

%INFO - ----------
%INFO - System IP750_E (IP750EX)
%INFO - IG-XL 3.50.40IP02, Build: 04.13.11.20.00
%INFO - Maintenance 7.60.40IP02, Build: 04.18.11.02.09
%INFO - ----------
- Systemwide functionality and continuity to slot 0
- Systemwide functionality and continuity to slot 1
- Starting BackPlane Fail Bus test
- Completed BackPlane Fail Bus test

- Completed Extra

%JOB_END - ****PASSED**** Systemwide tests at 11:51:25 AM

%JOB_START - Beginning CUB Module Check test on slot 18 at 11:51:36 AM on 1/17/2020
Workbook Rev V7.60.40IP02 DC1116 IG-XL Version: 3.50.40IP02 DIB: P/N 51745600
S/N xxxxxxx Rev 0901A

%INFO - ----------
%INFO - System IP750_E (IP750EX)
%INFO - IG-XL 3.50.40IP02, Build: 04.13.11.20.00
%INFO - Maintenance 7.60.40IP02, Build: 04.18.11.02.09
%INFO - ----------
- Testing CalCUB and CalDIB Leakage
- Completed Cal Dib Leakage Test
- Testing CalCUB Voltage Sources on CalDIB
- Beginning Cal DIB RawV Test on Slot18
- Completed Cal DIB RawV Test on Slot 18
- Beginning Cal Dib to BPMU Test on Slot 0
- Completed Cal Dib to BPMU Test on Slot 0
- Beginning Cal Dib to EXTERN Test on Slot 0
- Completed Cal Dib to EXTERN Test on Slot 0
- Testing CalDIB Utility Bit Relays using Channel Board Utility Bits for Slot 0
- Completed Cal Dib to UTIL Test on Slot 0
- Beginning Cal Dib RF Tree & Pogo Test

- Beginning Cal Dib to BPMU Test on Slot 1
- Completed Cal Dib to BPMU Test on Slot 1
- Beginning Cal Dib to EXTERN Test on Slot 1
- Completed Cal Dib to EXTERN Test on Slot 1
- Testing CalDIB Utility Bit Relays using Channel Board Utility Bits for Slot 1
- Completed Cal Dib to UTIL Test on Slot 1
- Beginning Cal Dib RF Tree & Pogo Test

- Beginning Cal DIB to DPS_FSG Test on Slot 22
- Completed Cal DIB to DPS_FSG Test on Slot 22
- Testing Device Ground Sense on CalDIB
- Completed DGS Test
- ****Completed CalDib Test****
- Start Compare Level Vol test
- Completed Compare Level Vol test
- Start Compare Level Voh test
- Completed Compare Level Voh test
- Start Drive_Level_test VIL
- Completed Drive_Level_test VIL
- Start Drive_Level_test VIH
- Completed Drive_Level_test VIH
- Beginning CalCub_Measure_Current using Bpmu in Slot 0
- Completed CalCub_Measure_Current

%JOB_END - ****PASSED**** CUB Module Check of slot 18 (S/N:xxxxxxxx) at 11:52:05 AM

%JOB_START - Beginning Channel_Board_DIB Module Check test on slot(s) 0,1 at 11:52:17 AM on
1/17/2020
Workbook Rev V7.60.40IP02 DC1116 IG-XL Version: 3.50.40IP02 DIB: P/N 51745600 S/N xxxxxxx Rev 0901A

%INFO - ----------
%INFO - System IP750_E (IP750EX)
%INFO - IG-XL 3.50.40IP02, Build: 04.13.11.20.00
%INFO - Maintenance 7.60.40IP02, Build: 04.18.11.02.09
%INFO - ----------
- Beginning ID PROM Check
- Channel Board in Slot 0: Serial #:C1 Rev Date:1142B
- TERM. Rider in Slot 0: Serial #:C1 Rev Date:838A
- Channel Board in Slot 1: Serial #:C1 Rev Date:1113B
- TERM. Rider in Slot 1: Serial #:C1 Rev Date:838A
- Finished ID-PROM Check on all slots
- Beginning CB200 DUT Continuity
- ...Testing Board in Slot 0
- ...Testing Board in Slot 1
- Finished CB200 DUT Continuity on all slots
- Beginning Ram Test
- Finished on all slots
- Beginning ChanRam Test
- Finished on all slots
- Beginning Period Generator test
- Starting Residue test
- Finished Residue test
- Starting Period Ram Single Mode Test
- Finished Period Ram Single Mode Test
- Starting Period Ram Dual Mode Test
- Finished Period Ram Dual Mode Test
- Starting Period Ram Quad Mode Test
- Finished Period Ram Quad Mode Test
- Starting Residue test
- Finished Residue test
- Starting Period Ram Single Mode Test
- Finished Period Ram Single Mode Test
- Starting Period Ram Dual Mode Test
- Finished Period Ram Dual Mode Test
- Starting Period Ram Quad Mode Test
- Finished Period Ram Quad Mode Test
- Finished on all slots
- Beginning HFMUX test
- HFMux 4 test passed for channel output 0
- HFMux 4 test passed for channel output 2
- HFMux 4 test passed for channel output 12
- HFMux 4 test passed for channel output 14
- HFMux 4 test passed for channel output 16
- HFMux 4 test passed for channel output 18
- HFMux 4 test passed for channel output 28
- HFMux 4 test passed for channel output 30

- HFMux 4 test passed for channel output 32
- HFMux 4 test passed for channel output 34
- HFMux 4 test passed for channel output 44
- HFMux 4 test passed for channel output 46
- HFMux 4 test passed for channel output 48
- HFMux 4 test passed for channel output 50
- HFMux 4 test passed for channel output 0
- HFMux 4 test passed for channel output 2
- HFMux 4 test passed for channel output 12
- HFMux 4 test passed for channel output 14
- HFMux 4 test passed for channel output 16
- HFMux 4 test passed for channel output 18
- HFMux 4 test passed for channel output 28
- HFMux 4 test passed for channel output 30
- HFMux 4 test passed for channel output 32
- HFMux 4 test passed for channel output 34
- HFMux 4 test passed for channel output 44
- HFMux 4 test passed for channel output 46
- HFMux 4 test passed for channel output 48
- HFMux 4 test passed for channel output 50
- Finished HFMUX test on all slots

- Beginning KeepAlive Test
- Testing Single Mode
- Continuing test: Verifies PG Enters KA
- Extended Mode KeepAlive Pattern Test Start
- Continuing test: Verifies PG Exit.
- Continuing test: Vector Number Set
- Completed KeepAlive test
- Testing Dual Mode
- Continuing test: Verifies PG Enters KA
- Normal Mode KeepAlive Pattern Test Start
- Continuing test: Verifies PG Exit.
- Continuing test: Vector Number Set
- Completed KeepAlive test
- Testing Quad Mode
- Continuing test: Verifies PG Enters KA
- Quad Mode KeepAlive Pattern Test Start
- Continuing test: Verifies PG Exit.
- Continuing test: Vector Number Set
- Completed KeepAlive test
- Testing Single Mode
- Continuing test: Verifies PG Enters KA
- Extended Mode KeepAlive Pattern Test Start
- Continuing test: Verifies PG Exit.
- Continuing test: Vector Number Set
- Completed KeepAlive test
- Testing Dual Mode
- Continuing test: Verifies PG Enters KA
- Normal Mode KeepAlive Pattern Test Start
- Continuing test: Verifies PG Exit.
- Continuing test: Vector Number Set

- Completed KeepAlive test
- Testing Quad Mode
- Continuing test: Verifies PG Enters KA
- Quad Mode KeepAlive Pattern Test Start
- Continuing test: Verifies PG Exit.
- Continuing test: Vector Number Set
- Completed KeepAlive test
- Finished KeepAlive on all slots

- Beginning PE Vt Third Level test
- Beginning Third Level test for VT = 0 Volts
- Beginning Third Level test for VT = 1 Volts
- Beginning Third Level test for VT = 2 Volts
- Beginning Third Level test for VT = 3 Volts
- Beginning Third Level test for VT = 4 Volts
- Beginning Third Level test for VT = 5 Volts
- Finished on all slots

- Starting High Voltage Channel Tests
- Testing Legacy HV Driver on slot 0
- Testing Fast HV PE Driver on slot 0
- Testing Legacy HV Driver on slot 1
- Testing Fast HV PE Driver on slot 1
- Finished High Voltage Channel Tests on all slots
- Beginning Split RAM Test test
- Started RsvmRlvm1_Normal Test
- Continuing RsvmRlvm1_Normal test.
- Completed RsvmRlvm1_Normal test.
- Started RsvmRlvm2_Normal Test
- Continuing RsvmRlvm2_Normal test.
- Completed RsvmRlvm2_Normal test.
- Started RsvmRlvm3_Normal Test
- Continuing RsvmRlvm3_Normal test.
- Continuing RsvmRlvm3_Normal test.
- Completed RsvmRlvm3_Normal test.
- Started RsvmRlvm4_Normal Test
- Continuing RsvmRlvm4_Normal test.
- Continuing RsvmRlvm4_Normal test.
- Continuing RsvmRlvm4_Normal test.
- Continuing RsvmRlvm4_Normal test.
- Completed RsvmRlvm4_Normal test.
- Started RsvmRlvm_Combo1_Normal Test
- Completed RsvmRlvm_Combo1_Normal test.
- Started LvmAddr1_Normal Test
- Completed LvmAddr1_Normal test.
- Started LvmErr1_Normal Test
- Completed LvmErr1_Normal test.
- Started LvmCallSvmSubr1_Normal Test
- Continuing LvmCallSvmSubr1_Normal test.
- Continuing LvmCallSvmSubr1_Normal test.
- Completed LvmCallSvmSubr1_Normal test.
- Started RsvmRlvm1_Extended Test

- Continuing RsvmRlvm1_Extended test.
- Completed RsvmRlvm1_Extended test.
- Started RsvmRlvm2_Extended Test
- Continuing RsvmRlvm2_Extended test.
- Completed RsvmRlvm2_Extended test.
- Started RsvmRlvm3_Extended Test
- Continuing RsvmRlvm3_Extended test.
- Continuing RsvmRlvm3_Extended test.
- Completed RsvmRlvm3_Extended test.
- Started RsvmRlvm4_Extended Test
- Continuing RsvmRlvm4_Extended test.
- Continuing RsvmRlvm4_Extended test.
- Continuing RsvmRlvm4_Extended test.
- Completed RsvmRlvm4_Extended test.
- Started RsvmRlvm_Combo1_Extended Test
- Completed RsvmRlvm_Combo1_Extended test.
- Started LvmAddr1_Extended Test
- Completed LvmAddr1_Extended test.
- Started LvmErr1_Ext Test
- Completed LvmErr1_Ext test.
- Started LvmCallSvmSubr1_Extended Test
- Continuing LvmCallSvmSubr1_Extended test.
- Continuing LvmCallSvmSubr1_Extended test.
- Continuing LvmCallSvmSubr1_Extended test.
- Continuing LvmCallSvmSubr1_Extended test.
- Continuing LvmCallSvmSubr1_Extended test.
- Completed LvmCallSvmSubr1_Extended test.
- Started RsvmRlvm1_Normal Test
- Continuing RsvmRlvm1_Normal test.
- Completed RsvmRlvm1_Normal test.
- Started RsvmRlvm2_Normal Test
- Continuing RsvmRlvm2_Normal test.
- Completed RsvmRlvm2_Normal test.
- Started RsvmRlvm3_Normal Test
- Continuing RsvmRlvm3_Normal test.
- Continuing RsvmRlvm3_Normal test.
- Completed RsvmRlvm3_Normal test.
- Started RsvmRlvm4_Normal Test
- Continuing RsvmRlvm4_Normal test.
- Continuing RsvmRlvm4_Normal test.
- Continuing RsvmRlvm4_Normal test.
- Continuing RsvmRlvm4_Normal test.
- Completed RsvmRlvm4_Normal test.
- Started RsvmRlvm_Combo1_Normal Test
- Completed RsvmRlvm_Combo1_Normal test.
- Started LvmAddr1_Normal Test
- Completed LvmAddr1_Normal test.
- Started LvmErr1_Normal Test
- Completed LvmErr1_Normal test.
- Started LvmCallSvmSubr1_Normal Test
- Continuing LvmCallSvmSubr1_Normal test.
- Continuing LvmCallSvmSubr1_Normal test.

- Completed LvmCallSvmSubr1_Normal test.
- Started RsvmRlvm1_Extended Test
- Continuing RsvmRlvm1_Extended test.
- Completed RsvmRlvm1_Extended test.
- Started RsvmRlvm2_Extended Test
- Continuing RsvmRlvm2_Extended test.
- Completed RsvmRlvm2_Extended test.
- Started RsvmRlvm3_Extended Test
- Continuing RsvmRlvm3_Extended test.
- Continuing RsvmRlvm3_Extended test.
- Completed RsvmRlvm3_Extended test.
- Started RsvmRlvm4_Extended Test
- Continuing RsvmRlvm4_Extended test.
- Continuing RsvmRlvm4_Extended test.
- Continuing RsvmRlvm4_Extended test.
- Completed RsvmRlvm4_Extended test.
- Started RsvmRlvm_Combo1_Extended Test
- Completed RsvmRlvm_Combo1_Extended test.
- Started LvmAddr1_Extended Test
- Completed LvmAddr1_Extended test.
- Started LvmErr1_Ext Test
- Completed LvmErr1_Ext test.
- Started LvmCallSvmSubr1_Extended Test
- Continuing LvmCallSvmSubr1_Extended test.
- Continuing LvmCallSvmSubr1_Extended test.
- Continuing LvmCallSvmSubr1_Extended test.
- Continuing LvmCallSvmSubr1_Extended test.
- Continuing LvmCallSvmSubr1_Extended test.
- Completed LvmCallSvmSubr1_Extended test.
- Finished on all slots
- Beginning MuxPin Test
- MuxPin Test MuxTime = 0.1
- MuxPin Test MuxTime = 0.3
- MuxPin Test MuxTime = 0.5
- MuxPin Test MuxTime = 0.7
- MuxPin Test MuxTime = 0.9
- MuxPin Test MuxTime = 0.1
- MuxPin Test MuxTime = 0.3
- MuxPin Test MuxTime = 0.5
- MuxPin Test MuxTime = 0.7
- MuxPin Test MuxTime = 0.9
- Finished MuxPin Tests on all slots

- Starting DownLoad tests for slot 0
- Starting PG SVM Download test
- PG Download test passed.
- Completed PG SVM Download test
- Completed DownLoad tests for slot 0
- Starting DownLoad tests for slot 1
- Starting PG SVM Download test
- PG Download test passed.
- Completed PG SVM Download test

- Completed DownLoad tests for slot 1
- Finished on all slots
- Beginning Scan Test test
- Starting Scan Test Stride of: 3
- Scan Test Stride Register on Chan 0 Reads: 3 PASSED
- Scan Test TG LVM Image - Stride of 3 Passed
- Scan Test Stride Register on Chan 16 Reads: 3 PASSED
- Scan Test TG LVM Image - Stride of 3 Passed
- Scan Test Stride Register on Chan 32 Reads: 3 PASSED
- Scan Test TG LVM Image - Stride of 3 Passed
- Scan Test Stride Register on Chan 48 Reads: 3 PASSED
- Scan Test TG LVM Image - Stride of 3 Passed
- Starting Scan Test Stride of: 4
- Scan Test Stride Register on Chan 0 Reads: 4 PASSED
- Scan Test TG LVM Image - Stride of 4 Passed
- Scan Test Stride Register on Chan 16 Reads: 4 PASSED
- Scan Test TG LVM Image - Stride of 4 Passed
- Scan Test Stride Register on Chan 32 Reads: 4 PASSED
- Scan Test TG LVM Image - Stride of 4 Passed
- Scan Test Stride Register on Chan 48 Reads: 4 PASSED
- Scan Test TG LVM Image - Stride of 4 Passed
- Starting Scan Test Stride of: 9
- Scan Test Stride Register on Chan 0 Reads: 10 PASSED
- Scan Test TG LVM Image - Stride of 9 Passed
- Scan Test Stride Register on Chan 16 Reads: 10 PASSED
- Scan Test TG LVM Image - Stride of 9 Passed
- Scan Test Stride Register on Chan 32 Reads: 10 PASSED
- Scan Test TG LVM Image - Stride of 9 Passed
- Scan Test Stride Register on Chan 48 Reads: 10 PASSED
- Scan Test TG LVM Image - Stride of 9 Passed
- Starting Scan Test Stride of: 12
- Scan Test Stride Register on Chan 0 Reads: 12 PASSED
- Scan Test TG LVM Image - Stride of 12 Passed
- Scan Test Stride Register on Chan 16 Reads: 12 PASSED
- Scan Test TG LVM Image - Stride of 12 Passed
- Scan Test Stride Register on Chan 32 Reads: 12 PASSED
- Scan Test TG LVM Image - Stride of 12 Passed
- Scan Test Stride Register on Chan 48 Reads: 12 PASSED
- Scan Test TG LVM Image - Stride of 12 Passed
- Starting Scan Pattern Burst Over ADB on slot 0
- Scan Test Scan Burst Lower ADB Bits Passed
- Scan Test Scan Burst Upper ADB Bits Passed
- Starting Scan Test Stride of: 3
- Scan Test Stride Register on Chan 0 Reads: 3 PASSED
- Scan Test TG LVM Image - Stride of 3 Passed
- Scan Test Stride Register on Chan 16 Reads: 3 PASSED
- Scan Test TG LVM Image - Stride of 3 Passed
- Scan Test Stride Register on Chan 32 Reads: 3 PASSED
- Scan Test TG LVM Image - Stride of 3 Passed
- Scan Test Stride Register on Chan 48 Reads: 3 PASSED
- Scan Test TG LVM Image - Stride of 3 Passed
- Starting Scan Test Stride of: 4

- Scan Test Stride Register on Chan 0 Reads: 4 PASSED
- Scan Test TG LVM Image - Stride of 4 Passed
- Scan Test Stride Register on Chan 16 Reads: 4 PASSED
- Scan Test TG LVM Image - Stride of 4 Passed
- Scan Test Stride Register on Chan 32 Reads: 4 PASSED
- Scan Test TG LVM Image - Stride of 4 Passed
- Scan Test Stride Register on Chan 48 Reads: 4 PASSED
- Scan Test TG LVM Image - Stride of 4 Passed
- Starting Scan Test Stride of: 9
- Scan Test Stride Register on Chan 0 Reads: 10 PASSED
- Scan Test TG LVM Image - Stride of 9 Passed
- Scan Test Stride Register on Chan 16 Reads: 10 PASSED
- Scan Test TG LVM Image - Stride of 9 Passed
- Scan Test Stride Register on Chan 32 Reads: 10 PASSED
- Scan Test TG LVM Image - Stride of 9 Passed
- Scan Test Stride Register on Chan 48 Reads: 10 PASSED
- Scan Test TG LVM Image - Stride of 9 Passed
- Starting Scan Test Stride of: 12
- Scan Test Stride Register on Chan 0 Reads: 12 PASSED
- Scan Test TG LVM Image - Stride of 12 Passed
- Scan Test Stride Register on Chan 16 Reads: 12 PASSED
- Scan Test TG LVM Image - Stride of 12 Passed
- Scan Test Stride Register on Chan 32 Reads: 12 PASSED
- Scan Test TG LVM Image - Stride of 12 Passed
- Scan Test Stride Register on Chan 48 Reads: 12 PASSED
- Scan Test TG LVM Image - Stride of 12 Passed
- Starting Scan Pattern Burst Over ADB on slot 1
- Scan Test Scan Burst Lower ADB Bits Passed
- Scan Test Scan Burst Upper ADB Bits Passed
- Finished on all slots
- Beginning SCIO Test
- Drive Burst SCIO Ones
- Drive Burst SCIO Zeros
- Receive Burst SCIO Ones
- Receive Burst SCIO Zeros
- Drive Burst SCIO Ones
- Drive Burst SCIO Zeros
- Receive Burst SCIO Ones
- Receive Burst SCIO Zeros
- Finished SCIO Test on all slots
- Starting DownLoad tests for slot 0
- Starting Extended Mode Download test
- Starting Edge Set RAM Download test
- Completed Edge Set RAM Download test
- Starting Format Map RAM Download test
- Completed Format Map RAM Download test
- Starting Format Set RAM Download test
- Completed Format Set RAM Download test
- Starting Tset Lookdown RAM Download test
- Completed Tset Lookdown RAM Download test
- Starting Misc Registers Download test
- Completed Misc Registers Download test

- Starting TG SVM Download test
- Completed TG SVM Download test
- Starting Quad Mode Download test
- Starting Edge Set RAM Download test
- Completed Edge Set RAM Download test
- Starting Format Map RAM Download test
- Completed Format Map RAM Download test
- Starting Format Set RAM Download test
- Completed Format Set RAM Download test
- Starting Tset Lookdown RAM Download test
- Completed Tset Lookdown RAM Download test
- Starting Misc Registers Download test
- Completed Misc Registers Download test
- Starting TG SVM Download test
- Completed TG SVM Download test
- Completed DownLoad tests for slot 0
- Starting DownLoad tests for slot 1
- Starting Extended Mode Download test
- Starting Edge Set RAM Download test
- Completed Edge Set RAM Download test
- Starting Format Map RAM Download test
- Completed Format Map RAM Download test
- Starting Format Set RAM Download test
- Completed Format Set RAM Download test
- Starting Tset Lookdown RAM Download test
- Completed Tset Lookdown RAM Download test
- Starting Misc Registers Download test
- Completed Misc Registers Download test
- Starting TG SVM Download test
- Completed TG SVM Download test
- Starting Quad Mode Download test
- Starting Edge Set RAM Download test
- Completed Edge Set RAM Download test
- Starting Format Map RAM Download test
- Completed Format Map RAM Download test
- Starting Format Set RAM Download test
- Completed Format Set RAM Download test
- Starting Tset Lookdown RAM Download test
- Completed Tset Lookdown RAM Download test
- Starting Misc Registers Download test
- Completed Misc Registers Download test
- Starting TG SVM Download test
- Completed TG SVM Download test
- Completed DownLoad tests for slot 1
- Finished on all slots
- Beginning PPMU FIMV
- PPMU FIMV IRange=50mA:Iforce=-25mA
- PPMU FIMV IRange=50mA:Iforce=0mA
- PPMU FIMV IRange=50mA:Iforce=25mA
- PPMU FIMV IRange=50mA:Iforce=40mA
- PPMU FIMV IRange=50mA:Iforce=50mA
- PPMU FIMV IRange=2mA:Iforce=-1.45mA

- PPMU FIMV IRange=2mA:Iforce=-1mA
- PPMU FIMV IRange=2mA:Iforce=0mA
- PPMU FIMV IRange=2mA:Iforce=1mA
- PPMU FIMV IRange=2mA:Iforce=2mA
- PPMU FIMV IRange=200uA:Iforce=-200uA
- PPMU FIMV IRange=200uA:Iforce=-100uA
- PPMU FIMV IRange=200uA:Iforce=0uA
- PPMU FIMV IRange=200uA:Iforce=100uA
- PPMU FIMV IRange=200uA:Iforce=200uA
- Finished PPMU FIMV
- Beginning PPMU FVMI
- PPMU FVMI Vforce=-1.5V Irange=2mA
- PPMU FVMI Vforce=-1V Irange=2mA
- PPMU FVMI Vforce=0V Irange=0.2mA
- PPMU FVMI Vforce=1V Irange=2mA
- PPMU FVMI Vforce=1.5V Irange=2mA
- PPMU FVMI Vforce=2V Irange=2mA
- PPMU FVMI Vforce=3V Irange=50mA
- PPMU FVMI Vforce=4V Irange=50mA
- PPMU FVMI Vforce=5V Irange=50mA
- PPMU FVMI Vforce=6V Irange=50mA
- Finished PPMU FVMI
- Starting MultiClock test
- Completed MultiClock test

- Beginning Frequency Counter test
- Completed Frequency Count test

- Beginning Levels Memory BIST
- Actual BIST Time for All boards = 0.171875secs
- Levels Memory BIST Passed on Slot: 1
- Levels Memory BIST Passed on Slot: 0
- Finished Levels Memory BIST on all slots
- Beginning Utility Bit test
- Completed Utility Bit test
- Beginning Utility Bit test
- Completed Utility Bit test
- Finished on all slots
- Starting Fail Bus test
- ...Testing Fail Bus on slot 0
- ...Testing Fail Bus on slot 1
- Finished on all slots
- Beginning Random Pattern test
- Starting Single Mode SVM Test
- Random Pattern Passed

- Random Pattern Passed

- Single Mode SVM Test Done
- Starting Single Mode LVM Test
- Random Pattern Passed

- Random Pattern Passed

- Single Mode LVM Test Done
- Starting Dual Mode SVM Test
- Random Pattern Passed

- Random Pattern Passed

- Dual Mode SVM Test Done
- Starting Dual Mode LVM Test
- Random Pattern Passed

- Random Pattern Passed

- Dual Mode LVM Test Done
- Starting Quad Mode SVM Test
- Random Pattern Passed

- Random Pattern Passed

- Quad Mode SVM Test Done
- Starting Quad Mode LVM Test
- Random Pattern Passed

- Random Pattern Passed

- Quad Mode LVM Test Done
- Finished on all slots
- Starting Board PMU test
- Completed Board PMU test
- Starting Board PMU test
- Completed Board PMU test
- Completed Channel_Board_DIB test on slot 1

%JOB_END - ****PASSED**** Channel_Board_DIB Module Check of slot(s) 0, 1 at 11:54:32 AM

- PASS slot 0 (S/N)
- PASS slot 1 (S/N)

%JOB_START - Beginning Relay_Board_Lower Module Check test on slot(s) 0,1 at 11:54:43 AM on
1/17/2020
Workbook Rev V7.60.40IP02 DC1116 IG-XL Version: 3.50.40IP02 DIB: P/N 51745600 S/N xxxxxxx Rev 0901A

%INFO - ----------
%INFO - System IP750_E (IP750EX)
%INFO - IG-XL 3.50.40IP02, Build: 04.13.11.20.00
%INFO - Maintenance 7.60.40IP02, Build: 04.18.11.02.09
%INFO - ----------
- Beginning Relay Brd Lower Chans
- Relay Brd Lower Chans - PE Close & BPMU Close slot0 - Passed

- Relay Brd Lower Chans - PE Close & BPMU Close slot1 - Passed
- Relay Brd Lower Chans - PE Open & BPMU Close slot0 - Passed
- Relay Brd Lower Chans - PE Open & BPMU Close slot1 - Passed
- Relay Brd Lower Chans - PE Close & BPMU Open slot0 - Passed
- Relay Brd Lower Chans - PE Close & BPMU Open slot1 - Passed
- Finished Relay Brd Lower Chans
- Completed Relay_Board_Lower test on slot 1

%JOB_END - ****PASSED**** Relay_Board_Lower Module Check of slot(s) 0, 1 at 11:54:47 AM
- PASS slot 0
- PASS slot 1

%JOB_START - Beginning Relay_Board_Upper Module Check test on slot(s) 0,1 at 11:54:58 AM on
1/17/2020
Workbook Rev V7.60.40IP02 DC1116 IG-XL Version: 3.50.40IP02 DIB: P/N 51745600 S/N xxxxxxx Rev 0901A

%INFO - ----------
%INFO - System IP750_E (IP750EX)
%INFO - IG-XL 3.50.40IP02, Build: 04.13.11.20.00
%INFO - Maintenance 7.60.40IP02, Build: 04.18.11.02.09
%INFO - ----------
- Beginning Relay Brd Upper Chans
- Relay Brd Upper Chans - PE Close & BPMU Close slot0 - Passed
- Relay Brd Upper Chans - PE Close & BPMU Close slot1 - Passed
- Relay Brd Upper Chans - PE Open & BPMU Close slot0 - Passed
- Relay Brd Upper Chans - PE Open & BPMU Close slot1 - Passed
- Relay Brd Upper Chans - PE Close & BPMU Open slot0 - Passed
- Relay Brd Upper Chans - PE Close & BPMU Open slot1 - Passed
- Finished Relay Brd Upper Chans
- Completed Relay_Board_Upper test on slot 1

%JOB_END - ****PASSED**** Relay_Board_Upper Module Check of slot(s) 0, 1 at 11:55:02 AM
- PASS slot 0
- PASS slot 1

%JOB_START - Beginning DPS_DIB Module Check test on slot 22 at 11:55:15 AM on 1/17/2020
Workbook Rev V7.60.40IP02 DC1116 IG-XL Version: 3.50.40IP02 DIB: P/N 51745600 S/N xxxxxxx Rev 0901A

%INFO - ----------
%INFO - System IP750_E (IP750EX)
%INFO - IG-XL 3.50.40IP02, Build: 04.13.11.20.00
%INFO - Maintenance 7.60.40IP02, Build: 04.18.11.02.09
%INFO - ----------
- The license of DPS_MOUT is not available.
- DPS_MOUT Check Skipped.

%JOB_END - ****PASSED**** DPS_DIB Module Check of slot 22 (S/N:) at 11:55:25 AM

%JOB_START - Beginning ICUA Module Check test on slot 2 at 11:55:37 AM on 1/17/2020
Workbook Rev V7.60.40IP02 DC1116 IG-XL Version: 3.50.40IP02 DIB: P/N 51745600 S/N xxxxxxx Rev 0901A

%INFO - ----------
%INFO - System IP750_E (IP750EX)
%INFO - IG-XL 3.50.40IP02, Build: 04.13.11.20.00
%INFO - Maintenance 7.60.40IP02, Build: 04.18.11.02.09
%INFO - ----------
- Starting dib_test
- ICUA-2 P/N:51742601 Rev:738B S/N:4
- %INFO -- ADM on ICUA-2 Chan0 Slot2, ADM P/N:51740520 Rev:735C S/N:
- %INFO -- ADM on ICUA-2 Chan1 Slot2, ADM P/N:51740520 Rev:735C S/N:
- %INFO -- ADM on ICUA-2 Chan2 Slot2, ADM P/N:51740520 Rev:735C S/N:
- %INFO -- ADM on ICUA-2 Chan3 Slot2, ADM P/N:51740520 Rev:735C S/N:
- ICUA-2 Relay board P/N:51742800 Rev:515C S/N:

- *** Start to test on Multi PC Environment ***
- [Check the existence of Giga-Channel on PCs]
- ImagePC#0
- [Overlap Check Giga-Channel NodeID on Image Processing PC]

- -- Check on Token Link Connection
- Starting PG_History_Ram
- Completed PG_History_Ram
- Starting PG_Svm_Ram
- Completed PG_Svm_Ram
- Starting PG_Scramble_Ram, ADSS
- Completed PG_Scramble_Ram
- Starting PG_Scramble_Ram, Tset
- Completed PG_Scramble_Ram
- Starting PG_LVM_BIST_Ram (up to 32 sec)
- Completed PG_LVM_BIST_Ram in 21.6 sec

- %INFO - LRS Off
- Starting TG Register Tests...
- Completed TG Register Tests
- Starting ICUA_TG_Period_Ram...
- Completed ICUA_TG_Period_Ram
- Starting ICUA_TG_Period_Map_Ram...
- Completed TG_Period_Map_Ram
- Starting TG_LVM_BIST_Ram (up to 32 sec)
- Completed TG_LVM_BIST_Ram in 10.8 sec
- Starting ICUA_TG_History_Ram
- Completed ICUA_TG_History_Ram
- Starting ICUA_TG_SVM_Ram
- Completed ICUA_TG_SVM_Ram
- Starting ICUA_TG_ADSS_Ram
- Completed ICUA_TG_ADSS_Ram
- Starting ICUA_TG_KeepAlive_Ram
- Completed ICUA_TG_KeepAlive_Ram

- Starting ICUA_TG_Tset_LkDwn_Ram
- Completed ICUA_TG_Tset_LkDwn_Ram
- Starting ICUA_TG_Edge_Ram
- Completed ICUA_TG_Edge_Ram
- Starting ICUA_TG_Format_Ram
- Completed ICUA_TG_Format_Ram
- Starting ICUA_TG_FormatLkDwn_Ram
- Completed ICUA_TG_FormatLkDwn_Ram
- %INFO - LRS On

- Starting ICUA MEM & MOV FPGA Registers...
- [ICUA Global IDL Register Check]
- [ICUA Channel Select IDL Register Check - Chan0]
- [Data Transfer and Giga Channel Control Register Check - Chan0]
- [ICUA Channel Select IDL Register Check - Chan1]
- [Data Transfer and Giga Channel Control Register Check - Chan1]
- [ICUA Channel Select IDL Register Check - Chan2]
- [Data Transfer and Giga Channel Control Register Check - Chan2]
- [ICUA Channel Select IDL Register Check - Chan3]
- [Data Transfer and Giga Channel Control Register Check - Chan3]
- [Data Transfer and Giga Channel Control Register Check]
- Completed ICUA MEM & MOV FPGA Registers

- Starting PPMU FPGA Registers
- Completed PPMU FPGA Registers

- Start ICUA board SDRAM/SVM Check
- Start ICUA SDRAM Check...
- [Data Uniqueness Test]
- [Address Uniqueness Test]
- [Data Dump Test(1K)]
- Completed ICUA SDRAM Check
- Start ICUA SVM Check...
- [Data Uniqueness Test]
- [Address Uniqueness Test]
- [Data Dump Test(1K)]
- Completed ICUA SVM Check
- Completed ICUA board SDRAM/SVM check

- Start ICUA board Download check...
- [1k words Download check]
- [Download SDRAM source address uniqueness check]
- [Download SVM destination address uniqueness check]
- [Up to 1k words Download check]
- Completed ICUA board Download check

- Starting Pin PMU Checker on ICUA...
- Performing PPMU force voltage tests...
- Completed PPMU force voltage tests
- Performing PPMU measure voltage tests...
- Completed PPMU measure voltage tests
- Performing PPMU force current tests...

- Completed PPMU force current tests
- Performing PPMU measure current tests...
- Completed PPMU measure current tests
- Performing PPMU list and ram tests...
- Completed PPMU list and ram tests
- Completed Pin PMU Checker on ICUA.

- Beginning Reference DAC test
- Completed Reference DAC test

- Starting State Bus test
- Statebus : Checking STB lines : Normal mode, 30MHz
- Statebus : Checking STB lines : Normal mode, 50MHz
- Statebus : Checking STB lines : Normal mode, 80MHz
- Statebus : Checking STB lines : Normal mode, 100MHz
- Statebus : Checking State number lines : Extended mode, 25MHz
- Statebus : Checking State number lines : Extended mode, 30MHz
- Statebus : Checking State number lines : Extended mode, 50MHz
- Completed State Bus test

- Starting KeepAlive Test, Extended Mode
- Continuing KeepAlive test
- Continuing KeepAlive test
- Completed KeepAlive test.
- Starting KeepAlive Test, Normal Mode
- Continuing KeepAlive test
- Continuing KeepAlive test
- Completed KeepAlive test.

- Start Capture Test [Checker Mode]...
- [Capture Test]
- [Capture Test(All Channel Capture)]
- [Accumulate Test]
- Completed Capture Test [Checker Mode]

- Start ADM Module Check....
- [Check ADM at ADM Channel = 0]
- [ADM Power Supply Voltage Check]
- [ADM Capture Bank check]
- [Offset Adjust check] (ADM 50M-A/D Converter Capture)
- [Offset Adjust check] (ADM 25M-A/D Converter Capture)
- [Input Voltage Range Test]
- [ADM Post-CDS Amp check]
- [ADM OffsetRemover Dac check]
- [ADM Optical Black Remover Dac check]
- [ADM CDS Circuit Test]
- [ADM LineClamp Circuit Test]
- [Check ADM at ADM Channel = 1]
- [ADM Power Supply Voltage Check]
- [ADM Capture Bank check]
- [Offset Adjust check] (ADM 50M-A/D Converter Capture)
- [Offset Adjust check] (ADM 25M-A/D Converter Capture)

- [Input Voltage Range Test]
- [ADM Post-CDS Amp check]
- [ADM OffsetRemover Dac check]
- [ADM Optical Black Remover Dac check]
- [ADM CDS Circuit Test]
- [ADM LineClamp Circuit Test]
- [Check ADM at ADM Channel = 2]
- [ADM Power Supply Voltage Check]
- [ADM Capture Bank check]
- [Offset Adjust check] (ADM 50M-A/D Converter Capture)
- [Offset Adjust check] (ADM 25M-A/D Converter Capture)
- [Input Voltage Range Test]
- [ADM Post-CDS Amp check]
- [ADM OffsetRemover Dac check]
- [ADM Optical Black Remover Dac check]
- [ADM CDS Circuit Test]
- [ADM LineClamp Circuit Test]
- [Check ADM at ADM Channel = 3]
- [ADM Power Supply Voltage Check]
- [ADM Capture Bank check]
- [Offset Adjust check] (ADM 50M-A/D Converter Capture)
- [Offset Adjust check] (ADM 25M-A/D Converter Capture)
- [Input Voltage Range Test]
- [ADM Post-CDS Amp check]
- [ADM OffsetRemover Dac check]
- [ADM Optical Black Remover Dac check]
- [ADM CDS Circuit Test]
- [ADM LineClamp Circuit Test]
- Completed ADM Module Check

- Beginning Utility Bit test...

- Completed Utility Bit test

- == Running with Image Processing PC(IMGPC0) only for Data Transfer Tests ==
- Start ICUA board Giga Channel data transfer check...
- [Acquire function check without averaging]
- 32-bit data transfer check
- [Acquire function check with averaging]
- -- 16bit GAIN bit check
- -- 24bit data divide check
- Completed ICUA board Giga Channel data transfer check

- Start APC-485T FIFO Check ...
- [Memory Size: 16777216 Bytes]
- Completed APC-485T FIFO Check

- Start APM-425T CheckSum Bit Check...
- 32-bit data transfer and all checksum bit check
- Completed APM-425T CheckSum Bit Check...

- Start ICUA board SDRAM stuck failure check...
- [SDRAM stuck @1 check(16M)]
- [--Check Bank A--]
- [--Check Bank B--]
- [--Check Bank C--]
- [SDRAM stuck @0 check(16M)]
- [--Check Bank C--]
- [--Check Bank B--]
- [--Check Bank A--]
- Completed ICUA board SDRAM stuck failure check

- Completed ICUA Module Check 114.8 sec

%JOB_END - ****PASSED**** ICUA Module Check of slot 2 (S/N:) at 11:57:32 AM

%JOB_START - Beginning APMU Module Check test on slot 5 at 11:57:45 AM on 1/17/2020
Workbook Rev V7.60.40IP02 DC1116 IG-XL Version: 3.50.40IP02 DIB: P/N 51745600 S/N xxxxxxx Rev 0901A

%INFO - ----------
%INFO - System IP750_E (IP750EX)
%INFO - IG-XL 3.50.40IP02, Build: 04.13.11.20.00
%INFO - Maintenance 7.60.40IP02, Build: 04.18.11.02.09
%INFO - ----------
- Starting APMU PG test
- Starting PG_History_Ram
- Completed PG_History_Ram
- Starting PG_Svm_Ram
- Completed PG_Svm_Ram
- Starting PG_Scramble_Ram, ADSS
- Completed PG_Scramble_Ram
- Starting PG_Scramble_Ram, Tset
- Completed PG_Scramble_Ram
- Starting PG_LVM_BIST_Ram (up to 32 sec)
- Completed PG_LVM_BIST_Ram in 21.6 sec
- Completed APMU PG test
-
- Starting APMU IDPROM test
- APMU Mother Board - P/N:51740001 Rev:1012A S/N: xxxxxxxx
- APMU Relay Board - P/N:51740200 Rev:2060 S/N: 2
- APMU Rider Board - P/N:51740100 Rev:5200 S/N: 25
- APMU Rider Board - P/N:51740100 Rev:5200 S/N: 25
- APMU Rider Board - P/N:51740100 Rev:5200 S/N: 25
- APMU Rider Board - P/N:51740100 Rev:5200 S/N: 25
- APMU Rider Board - P/N:51740100 Rev:5200 S/N: 25
- APMU Rider Board - P/N:51740100 Rev:5200 S/N: 25
- APMU Rider Board - P/N:51740100 Rev:5200 S/N: 24
- APMU Rider Board - P/N:51740100 Rev:5200 S/N: 25
- Completed APMU IDPROM test
-
- Starting APMU Register test
- Starting APMU Misc FPGA Register test

- Completed APMU Misc FPGA Register test
- Starting APMU Control FPGA Register test
- Completed APMU Control FPGA Register test
- Completed APMU Register test
-
- Starting APMU Thermal meter test
- Completed APMU Thermal meter test
-
- Starting APMU Voltages test
- Completed APMU Voltages test
-
- Start APMU Reference DAC test
- Complete APMU Reference DAC test
-
- Starting APMU Relay test
- Starting -VMBUS_H- test
- Completed -VMBUS_H- test
- Starting -VMBUS_L- test
- Completed -VMBUS_L- test
- Starting -CALBUS_HS- test
- Completed -CALBUS_HS- test
- Starting -CalBUS resistor- test
- Completed -CalBUS resistor- test
- Starting -HF_OUT- test
- Completed -HF_OUT- test
- Starting -GNG_HF- test
- Completed -GNG_HF- test
- Starting -Force and Sense setting- test
- Completed -Force and Sense setting- test
- Completed APMU Relay test

- Starting APMU Analog function test
- Starting -Gate Control- test
- Completed -Gate Control- test
- Starting -Parallel Site- test
- Completed -Parallel Site- test
- Starting -Differential Voltage Meter- test
- Completed -Differential Voltage Meter- test
- Starting -MV mode- test
- Completed -MV mode- test
- Starting -FV mode- test
- Completed -FV mode- test
- Starting -MI mode- test
- Completed -MI mode- test
- Starting -FI mode- test
- Completed -FI mode- test
- Starting -Clamp I mode- test
- Completed -Clamp I mode- test
- Starting -Clamp V mode- test
- Completed -Clamp V mode- test
- Starting -Gang_FV(8ch) mode- test
- Completed -Gang_FV(8ch) mode- test

- Starting -Gang_FI(8ch) mode- test
- Completed -Gang_FI(8ch) mode- test
- Starting -Gang_FV(2ch) mode- test
- Completed -Gang_FV(2ch) mode- test
- Starting -Gang_FI(2ch) mode- test
- Completed -Gang_FI(2ch) mode- test
- Starting -DGS Test-
- Completed -DGS Test-
- Completed APMU Analog function test

- Starting APMU Memory test
- Starting APMU Misc FPGA -Relay Data Memory- test
- Completed APMU Misc FPGA -Relay Data Memory- test
- Starting APMU Misc FPGA -Volt Meter Memory- test
- Completed APMU Misc FPGA -Volt Meter Memory- test
- Starting APMU Control FPGA -Source/Capture Memory- test
- Starting FPGA_0
- Completed FPGA_0
- Starting FPGA_1
- Completed FPGA_1
- Starting FPGA_2
- Completed FPGA_2
- Starting FPGA_3
- Completed FPGA_3
- Starting FPGA_4
- Completed FPGA_4
- Starting FPGA_5
- Completed FPGA_5
- Starting FPGA_6
- Completed FPGA_6
- Starting FPGA_7
- Completed FPGA_7
- Completed APMU Control FPGA -Source/Capture Memory- test
- Completed APMU Memory test
-

%JOB_END - ****PASSED**** APMU Module Check of slot 5 (S/N:xxxxxxxx) at 12:00:02 PM

%JOB_START - Beginning Channel_Board Performance Verification test on slot(s) 0,1 at 12:07:02 PM
on 1/17/2020
Workbook Rev V7.60.40IP02 DC1116 IG-XL Version: 3.50.40IP02 DIB: P/N 51745600 S/N Rev 0901A

%INFO - ----------
%INFO - System IP750_ (IP750EX)
%INFO - IG-XL 3.50.40IP02, Build: 04.13.11.20.00
%INFO - Maintenance 7.60.40IP02, Build: 04.18.11.02.09
%INFO - ----------
- Beginning ID PROM Check
- Channel Board in Slot 0: Serial #:C156F35 Rev Date:1142B

- TERM. Rider in Slot 0: Serial #:C184A1B Rev Date:838A
- Channel Board in Slot 1: Serial #:C15686F Rev Date:1113B
- TERM. Rider in Slot 1: Serial #:C17D0E8 Rev Date:838A
- Finished ID-PROM Check on all slots
- Starting DCPV on slot 0
- Performing VIH/VIL level tests... at DGS=0mV
- Performing IOH/IOL level tests... at DGS=0mV
- Performing VT level tests... at DGS=0mV
- Performing Clamp level tests... at DGS=0mV
- Performing VOH/VOL level tests... at DGS=0mV
- Performing PPMU force voltage tests... at DGS=0mV
- Performing PPMU measure voltage tests... at DGS=0mV
- Performing PPMU force current tests... at DGS=0mV
- Performing PPMU measure current tests... DGS=0mV
- Performing Legacy High Voltage Channel level tests...
- Performing Fast High Voltage DC Level Tests...
- Starting BPMU Performance Verification on slot 0, DGS= 78.201 uV
- Verifying BPMU Forced Voltage Accuracy
- Verifying BPMU Voltage Measure Accuracy
- Verifying BPMU Forced Current Accuracy
- Verifying BPMU Current Measure Accuracy
- Verifying BPMU Voltage Clamping Accuracy
- Verifying BPMU Current Clamping Accuracy

- Finished BPMU Performance Verification on slot 0

- Finished DCPV on slot 0
- Starting DCPV on slot 1
- Performing VIH/VIL level tests... at DGS=0mV
- Performing IOH/IOL level tests... at DGS=0mV
- Performing VT level tests... at DGS=0mV
- Performing Clamp level tests... at DGS=0mV
- Performing VOH/VOL level tests... at DGS=0mV
- Performing PPMU force voltage tests... at DGS=0mV
- Performing PPMU measure voltage tests... at DGS=0mV
- Performing PPMU force current tests... at DGS=0mV
- Performing PPMU measure current tests... DGS=0mV
- Performing Legacy High Voltage Channel level tests...
- Performing Fast High Voltage DC Level Tests...
- Starting BPMU Performance Verification on slot 1, DGS= 2.571 mV
- Verifying BPMU Forced Voltage Accuracy
- Verifying BPMU Voltage Measure Accuracy
- Verifying BPMU Forced Current Accuracy
- Verifying BPMU Current Measure Accuracy
- Verifying BPMU Voltage Clamping Accuracy
- Verifying BPMU Current Clamping Accuracy

- Finished BPMU Performance Verification on slot 1

- Finished DCPV on slot 1
- All Tests Finished

%JOB_END - ****PASSED**** Channel_Board Performance Verification of slot(s) 0, 1 at 12:23:34 PM
- PASS slot 0 (S/N)
- PASS slot 1 (S/N)

%JOB_START - Beginning DPS_DIB Performance Verification test on slot 22 at 12:23:47 PM on 1/17/2020
Workbook Rev V7.60.40IP02 DC1116 IG-XL Version: 3.50.40IP02 DIB: P/N 51745600 S/N 3 Rev 0901A

%INFO - ----------
%INFO - System IP750_ (IP750EX)
%INFO - IG-XL 3.50.40IP02, Build: 04.13.11.20.00
%INFO - Maintenance 7.60.40IP02, Build: 04.18.11.02.09
%INFO - ----------
- Starting DPS Performance Verification on slot 22

- Verifying DPS Voltage Accuracy
- Verifying DPS Current Limit Accuracy
- Verifying DPS Current Measure Accuracy
- Channel 0
- Channel 1
- Channel 2
- Channel 3
- Channel 4
- Channel 5
- Channel 6
- Channel 7
- The license of DPS_MOUT is not available.
- DPS_MOUT Check Skipped.

- Finished DPS Performance Verification on slot 22

%JOB_END - ****PASSED**** DPS_DIB Performance Verification of slot 22 (S/N:C) at 12:24:18 PM

%JOB_START - Beginning APMU Performance Verification test on slot 5 at 12:24:30 PM on 1/17/2020
Workbook Rev V7.60.40IP02 DC1116 IG-XL Version: 3.50.40IP02 DIB: P/N 51745600 S/N Rev 0901A

%INFO - ----------
%INFO - System IP750_ (IP750EX)
%INFO - IG-XL 3.50.40IP02, Build: 04.13.11.20.00
%INFO - Maintenance 7.60.40IP02, Build: 04.18.11.02.09
%INFO - ----------
- Starting APMU Performance Verification on slot 5
- Starting APMU IDPROM test
- APMU Mother Board - P/N:51740001 Rev:1012A S/N:
- APMU Relay Board - P/N:51740200 Rev:2060 S/N: 2
- APMU Rider Board - P/N:51740100 Rev:5200 S/N: 2

- APMU Rider Board - P/N:51740100 Rev:5200 S/N: 2
- APMU Rider Board - P/N:51740100 Rev:5200 S/N: 2
- APMU Rider Board - P/N:51740100 Rev:5200 S/N: 2
- APMU Rider Board - P/N:51740100 Rev:5200 S/N: 2
- APMU Rider Board - P/N:51740100 Rev:5200 S/N: 2
- APMU Rider Board - P/N:51740100 Rev:5200 S/N: 2
- APMU Rider Board - P/N:51740100 Rev:5200 S/N: 2
- Completed APMU IDPROM test
-
- Completed APMU REFDATA Load
-
- Verifying APMU VREF Offset Accuracy
- Verifying APMU Differential Voltmeter Accuracy
- Verifying APMU Voltage Measure Accuracy
- Verifying APMU Force Current/Voltage Measure Accuracy
- Verifying APMU Force Voltage Accuracy
- Verifying APMU Current Measure 200nA Accuracy
- Verifying APMU Current Measure Accuracy
- Verifying APMU Force Current Accuracy
- Verifying APMU Current Clamp Accuracy
- Verifying APMU Voltage Clamp Accuracy
- Verifying APMU Ganged Force Voltage Accuracy
- Verifying APMU Ganged Force Current Accuracy
-
- Finished APMU Performance Verification on slot 5
-

%JOB_END - ****PASSED**** APMU Performance Verification of slot 5 (S/N:) at 12:27:18 PM

%JOB_START - Beginning ICUA Performance Verification test on slot 2 at 12:27:31 PM on 1/17/2020
Workbook Rev V7.60.40IP02 DC1116 IG-XL Version: 3.50.40IP02 DIB: P/N 51745600 S/N Rev 0901A

%INFO - ----------
%INFO - System IP750_ (IP750EX)
%INFO - IG-XL 3.50.40IP02, Build: 04.13.11.20.00
%INFO - Maintenance 7.60.40IP02, Build: 04.18.11.02.09
%INFO - ----------
- Starting dib_test
- ICUA-2 P/N:51742601 Rev:738B S/N:
- %INFO -- ADM on ICUA-2 Chan0 Slot2, ADM P/N:51740520 Rev:735C S/N:
- %INFO -- ADM on ICUA-2 Chan1 Slot2, ADM P/N:51740520 Rev:735C S/N:
- %INFO -- ADM on ICUA-2 Chan2 Slot2, ADM P/N:51740520 Rev:735C S/N:
- %INFO -- ADM on ICUA-2 Chan3 Slot2, ADM P/N:51740520 Rev:735C S/N:
- ICUA-2 Relay board P/N:51742800 Rev:515C S/N:

- *** Start to test on Multi PC Environment ***

- -- Check on Token Link Connection
- [Performance Check ADM at ICUA Chan 0]

- [ADM Power Supply Voltage Check]

- [ADM InputRange Performance Check](A/D Converter 25MHz)
- -- Voltage Range = 8V --
- -- Voltage Range = 4V --
- -- Voltage Range = 2V --
- -- Voltage Range = 1V --
- -- Voltage Range = 500mV --
- -- Voltage Range = 200mV --
- -- Voltage Range = 100mV --
- -- Voltage Range = 50mV --
- -- Voltage Range = 20mV --
- -- Voltage Range = 10mV --

- [ADM InputRange Performance Check](A/D Converter 50MHz)
- -- Voltage Range = 8V --
- -- Voltage Range = 4V --
- -- Voltage Range = 2V --
- -- Voltage Range = 1V --
- -- Voltage Range = 500mV --
- -- Voltage Range = 200mV --
- -- Voltage Range = 100mV --
- -- Voltage Range = 50mV --
- -- Voltage Range = 20mV --
- -- Voltage Range = 10mV --

- [ADM PostAmp Performance Check]
- (A/D Converter 25MHz)

- [ADM PostAmp Performance Check]
- (A/D Converter 50MHz)

- [ADM Offset D/A Converter Performance Check]
- (A/D Converter 25MHz)

- [ADM Offset D/A Converter Performance Check]
- (A/D Converter 50MHz)

- [ADM OpticalBlackRemover D/A Converter Performance Check]
- (A/D Converter 25MHz)

- [ADM OpticalBlackRemover D/A Converter Performance Check]
- (A/D Converter 50MHz)

- [ADM A/D Converter-25M Check]
- @25MHz
- @10MHz
- @5MHz
- @1MHz
- @500kHz

- [ADM A/D Converter-50M Check]

- @10MHz
- @25MHz
- @50MHz

- [ADM CDS Circuit Test]
- @10MHz(A/D Converter 25MHz)
- @5MHz(A/D Converter 25MHz)
- @1MHz(A/D Converter 25MHz)
- @500kHz(A/D Converter 25MHz)
- @100kHz(A/D Converter 25MHz)

- [ADM CDS Circuit Test]
- @10MHz(A/D Converter 50MHz)
- @25MHz(A/D Converter 50MHz)
- @50MHz(A/D Converter 50MHz)

- [ADM LineClamp Circuit Performance Test]
- @1MHz(A/D Converter 25MHz)
- @2MHz(A/D Converter 25MHz)

- [ADM Ground Level Noise Check](A/D Converter 25MHz)

- [ADM Ground Level Noise Check](A/D Converter 25MHz)
- (CDS On)

- [ADM Ground Level Noise Check](A/D Converter 50MHz)

- [ADM Ground Level Noise Check](A/D Converter 50MHz)
- (CDS On)

- [Performance Check ADM at ICUA Chan 1]

- [ADM Power Supply Voltage Check]

- [ADM InputRange Performance Check](A/D Converter 25MHz)
- -- Voltage Range = 8V --
- -- Voltage Range = 4V --
- -- Voltage Range = 2V --
- -- Voltage Range = 1V --
- -- Voltage Range = 500mV --
- -- Voltage Range = 200mV --
- -- Voltage Range = 100mV --
- -- Voltage Range = 50mV --
- -- Voltage Range = 20mV --
- -- Voltage Range = 10mV --

- [ADM InputRange Performance Check](A/D Converter 50MHz)
- -- Voltage Range = 8V --
- -- Voltage Range = 4V --
- -- Voltage Range = 2V --
- -- Voltage Range = 1V --
- -- Voltage Range = 500mV --

- -- Voltage Range = 200mV --
- -- Voltage Range = 100mV --
- -- Voltage Range = 50mV --
- -- Voltage Range = 20mV --
- -- Voltage Range = 10mV --

- [ADM PostAmp Performance Check]
- (A/D Converter 25MHz)

- [ADM PostAmp Performance Check]
- (A/D Converter 50MHz)

- [ADM Offset D/A Converter Performance Check]
- (A/D Converter 25MHz)

- [ADM Offset D/A Converter Performance Check]
- (A/D Converter 50MHz)

- [ADM OpticalBlackRemover D/A Converter Performance Check]
- (A/D Converter 25MHz)

- [ADM OpticalBlackRemover D/A Converter Performance Check]
- (A/D Converter 50MHz)

- [ADM A/D Converter-25M Check]
- @25MHz
- @10MHz
- @5MHz
- @1MHz
- @500kHz

- [ADM A/D Converter-50M Check]
- @10MHz
- @25MHz
- @50MHz

- [ADM CDS Circuit Test]
- @10MHz(A/D Converter 25MHz)
- @5MHz(A/D Converter 25MHz)
- @1MHz(A/D Converter 25MHz)
- @500kHz(A/D Converter 25MHz)
- @100kHz(A/D Converter 25MHz)

- [ADM CDS Circuit Test]
- @10MHz(A/D Converter 50MHz)
- @25MHz(A/D Converter 50MHz)
- @50MHz(A/D Converter 50MHz)

- [ADM LineClamp Circuit Performance Test]
- @1MHz(A/D Converter 25MHz)
- @2MHz(A/D Converter 25MHz)

- [ADM Ground Level Noise Check](A/D Converter 25MHz)

- [ADM Ground Level Noise Check](A/D Converter 25MHz)
- (CDS On)

- [ADM Ground Level Noise Check](A/D Converter 50MHz)

- [ADM Ground Level Noise Check](A/D Converter 50MHz)
- (CDS On)

- [Performance Check ADM at ICUA Chan 2]

- [ADM Power Supply Voltage Check]

- [ADM InputRange Performance Check](A/D Converter 25MHz)
- -- Voltage Range = 8V --
- -- Voltage Range = 4V --
- -- Voltage Range = 2V --
- -- Voltage Range = 1V --
- -- Voltage Range = 500mV --
- -- Voltage Range = 200mV --
- -- Voltage Range = 100mV --
- -- Voltage Range = 50mV --
- -- Voltage Range = 20mV --
- -- Voltage Range = 10mV --

- [ADM InputRange Performance Check](A/D Converter 50MHz)
- -- Voltage Range = 8V --
- -- Voltage Range = 4V --
- -- Voltage Range = 2V --
- -- Voltage Range = 1V --
- -- Voltage Range = 500mV --
- -- Voltage Range = 200mV --
- -- Voltage Range = 100mV --
- -- Voltage Range = 50mV --
- -- Voltage Range = 20mV --
- -- Voltage Range = 10mV --

- [ADM PostAmp Performance Check]
- (A/D Converter 25MHz)

- [ADM PostAmp Performance Check]
- (A/D Converter 50MHz)

- [ADM Offset D/A Converter Performance Check]
- (A/D Converter 25MHz)

- [ADM Offset D/A Converter Performance Check]
- (A/D Converter 50MHz)

- [ADM OpticalBlackRemover D/A Converter Performance Check]
- (A/D Converter 25MHz)

- [ADM OpticalBlackRemover D/A Converter Performance Check]
- (A/D Converter 50MHz)

- [ADM A/D Converter-25M Check]
- @25MHz
- @10MHz
- @5MHz
- @1MHz
- @500kHz

- [ADM A/D Converter-50M Check]
- @10MHz
- @25MHz
- @50MHz

- [ADM CDS Circuit Test]
- @10MHz(A/D Converter 25MHz)
- @5MHz(A/D Converter 25MHz)
- @1MHz(A/D Converter 25MHz)
- @500kHz(A/D Converter 25MHz)
- @100kHz(A/D Converter 25MHz)

- [ADM CDS Circuit Test]
- @10MHz(A/D Converter 50MHz)
- @25MHz(A/D Converter 50MHz)
- @50MHz(A/D Converter 50MHz)

- [ADM LineClamp Circuit Performance Test]
- @1MHz(A/D Converter 25MHz)
- @2MHz(A/D Converter 25MHz)

- [ADM Ground Level Noise Check](A/D Converter 25MHz)

- [ADM Ground Level Noise Check](A/D Converter 25MHz)
- (CDS On)

- [ADM Ground Level Noise Check](A/D Converter 50MHz)

- [ADM Ground Level Noise Check](A/D Converter 50MHz)
- (CDS On)

- [Performance Check ADM at ICUA Chan 3]

- [ADM Power Supply Voltage Check]

- [ADM InputRange Performance Check](A/D Converter 25MHz)
- -- Voltage Range = 8V --
- -- Voltage Range = 4V --
- -- Voltage Range = 2V --
- -- Voltage Range = 1V --
- -- Voltage Range = 500mV --

- -- Voltage Range = 200mV --
- -- Voltage Range = 100mV --
- -- Voltage Range = 50mV --
- -- Voltage Range = 20mV --
- -- Voltage Range = 10mV --

- [ADM InputRange Performance Check](A/D Converter 50MHz)
- -- Voltage Range = 8V --
- -- Voltage Range = 4V --
- -- Voltage Range = 2V --
- -- Voltage Range = 1V --
- -- Voltage Range = 500mV --
- -- Voltage Range = 200mV --
- -- Voltage Range = 100mV --
- -- Voltage Range = 50mV --
- -- Voltage Range = 20mV --
- -- Voltage Range = 10mV --

- [ADM PostAmp Performance Check]
- (A/D Converter 25MHz)

- [ADM PostAmp Performance Check]
- (A/D Converter 50MHz)

- [ADM Offset D/A Converter Performance Check]
- (A/D Converter 25MHz)

- [ADM Offset D/A Converter Performance Check]
- (A/D Converter 50MHz)

- [ADM OpticalBlackRemover D/A Converter Performance Check]
- (A/D Converter 25MHz)

- [ADM OpticalBlackRemover D/A Converter Performance Check]
- (A/D Converter 50MHz)

- [ADM A/D Converter-25M Check]
- @25MHz
- @10MHz
- @5MHz
- @1MHz
- @500kHz

- [ADM A/D Converter-50M Check]
- @10MHz
- @25MHz
- @50MHz

- [ADM CDS Circuit Test]
- @10MHz(A/D Converter 25MHz)
- @5MHz(A/D Converter 25MHz)
- @1MHz(A/D Converter 25MHz)

- @500kHz(A/D Converter 25MHz)
- @100kHz(A/D Converter 25MHz)

- [ADM CDS Circuit Test]
- @10MHz(A/D Converter 50MHz)
- @25MHz(A/D Converter 50MHz)
- @50MHz(A/D Converter 50MHz)

- [ADM LineClamp Circuit Performance Test]
- @1MHz(A/D Converter 25MHz)
- @2MHz(A/D Converter 25MHz)

- [ADM Ground Level Noise Check](A/D Converter 25MHz)

- [ADM Ground Level Noise Check](A/D Converter 25MHz)
- (CDS On)

- [ADM Ground Level Noise Check](A/D Converter 50MHz)

- [ADM Ground Level Noise Check](A/D Converter 50MHz)
- (CDS On)

- Starting Pin PMU Checker on ICUA...
- Performing PPMU force voltage tests...
- Completed PPMU force voltage tests
- Performing PPMU measure voltage tests...
- Completed PPMU measure voltage tests
- Performing PPMU force current tests...
- Completed PPMU force current tests
- Performing PPMU measure current tests...
- Completed PPMU measure current tests
- Completed Pin PMU Checker on ICUA.

- Completed ICUA Performance Check 137.6 sec

%JOB_END - ****PASSED**** ICUA Performance Verification of slot 2 (S/N:) at 12:29:48 PM

%JOB_START - Beginning PCIT Quick Check test on slot 0 at 12:02:00 PM on 1/17/2020
Workbook Rev V7.60.40IP02 DC1116 IG-XL Version: 3.50.40IP02 DIB: P/N 51745600 S/N Rev 0901A

%INFO - ----------
%INFO - System IP750_xxxE (IP750EX)
%INFO - IG-XL 3.50.40IP02, Build: 04.13.11.20.00
%INFO - Maintenance 7.60.40IP02, Build: 04.18.11.02.09
%INFO - ----------
- PCIT CARD INFORMATION:
Part Number: 605-452-21
Serial Number: xxx
Revision Date: 1049A
TCIT FPGA Version: 20101005

- Starting PCIT Register test
- Completed PCIT Register test
- Starting PCIT Free Running Timer test
- Completed PCIT Free Running Timer test
- Starting PCIT Retriggerable Timer 1 test
- Completed PCIT Retriggerable Timer 1 test
- Starting PCIT Retriggerable Timer 2 test
- Completed PCIT Retriggerable Timer 2 test
- Starting TCIT FPGA Version test
- Completed TCIT FPGA Version test
- Starting PCIT DMA Test to CUB PG_History_Ram test using DMA mode
- Test with DMA bypass = TRUE
- Test with DMA bypass = FALSE
- Completed PCIT DMA Test to CUB PG_History_Ram test using DMA mode

%JOB_END - ****PASSED**** PCIT Quick Check of slot 18 (S/N:xxx) at 12:02:13 PM

%JOB_START - Beginning CUB Quick Check test on slot 18 at 12:02:26 PM on 1/17/2020
Workbook Rev V7.60.40IP02 DC1116 IG-XL Version: 3.50.40IP02 DIB: P/N 51745600 S/N xxx Rev 0901A

%INFO - ----------
%INFO - System IP750_xxxE (IP750EX)
%INFO - IG-XL 3.50.40IP02, Build: 04.13.11.20.00
%INFO - Maintenance 7.60.40IP02, Build: 04.18.11.02.09
%INFO - ----------
- Starting DIB Power Tests
- Completed DIB Power Tests
- Starting System Fan Checks
- Completed System Fan Checks
- Starting PG_History_Ram
- Completed PG_History_Ram
- Starting PG_Svm_Ram
- Completed PG_Svm_Ram
- Starting PG_History_Ram using DMA mode
- Completed PG_History_Ram using DMA mode
- Starting PG_Svm_Ram using DMA mode
- Completed PG_Svm_Ram using DMA mode
- Starting PG_Scramble_Ram, ADSS
- Completed PG_Scramble_Ram
- Starting PG_Scramble_Ram, Tset
- Completed PG_Scramble_Ram
- Skipping PG_LVM_BIST_Ram
- Beginning Qck_Register Test
- Completed Qck_Register Test
- Starting CalCub_TG_Register Tests
- LRS Off
- LRS On
- Completed CalCub_TG_Register Tests
- Started IdProm Test
- Completed IdProm Test

- Beginning Force Voltage Test
- Completed Force Voltage Test
- Beginning TestRefToDac
- Completed TestRefToDac
- Starting the CalCubSLITest
- Completed the CalCubSLITest

%JOB_END - ****PASSED**** CUB Quick Check of slot 18 (S/N:C) at 12:02:36 PM

- Beginning Channel_Board test on all CB200 slots

%JOB_START - Beginning Channel_Board Quick Check test on slot(s) 0,1 at 12:02:49 PM on 1/17/2020

Workbook Rev V7.60.40IP02 DC1116 IG-XL Version: 3.50.40IP02 DIB: P/N 51745600 S/N xxx Rev 0901A

%INFO - ----------
%INFO - System IP750_xxxE (IP750EX)
%INFO - IG-XL 3.50.40IP02, Build: 04.13.11.20.00
%INFO - Maintenance 7.60.40IP02, Build: 04.18.11.02.09
%INFO - ----------
- Beginning ID PROM Check
- Channel Board in Slot 0: Serial #:C Rev Date:1142B
- TERM. Rider in Slot 0: Serial #:C Rev Date:838A
- Channel Board in Slot 1: Serial #:C Rev Date:1113B
- TERM. Rider in Slot 1: Serial #:C Rev Date:838A
- Finished ID-PROM Check on all slots
- Checking Board Temperatures
- Beginning CB200 Register Tests
- Testing slot 0
- Starting PG register tests
- *** PG Register Tests on Slot 0 passed
- Starting TG register tests
- *** TG 1 channel 0 on Slot 0 passed
- *** TG 1 channel 1 on Slot 0 passed
- *** TG 1 channel 2 on Slot 0 passed
- *** TG 1 channel 3 on Slot 0 passed
- *** TG 2 channel 4 on Slot 0 passed
- *** TG 2 channel 5 on Slot 0 passed
- *** TG 2 channel 6 on Slot 0 passed
- *** TG 2 channel 7 on Slot 0 passed
- *** TG 3 channel 8 on Slot 0 passed
- *** TG 3 channel 9 on Slot 0 passed
- *** TG 3 channel 10 on Slot 0 passed
- *** TG 3 channel 11 on Slot 0 passed
- *** TG 4 channel 12 on Slot 0 passed
- *** TG 4 channel 13 on Slot 0 passed
- *** TG 4 channel 14 on Slot 0 passed
- *** TG 4 channel 15 on Slot 0 passed
- *** TG 5 channel 16 on Slot 0 passed
- *** TG 5 channel 17 on Slot 0 passed
- *** TG 5 channel 18 on Slot 0 passed
- *** TG 5 channel 19 on Slot 0 passed

- *** TG 6 channel 20 on Slot 0 passed
- *** TG 6 channel 21 on Slot 0 passed
- *** TG 6 channel 22 on Slot 0 passed
- *** TG 6 channel 23 on Slot 0 passed
- *** TG 7 channel 24 on Slot 0 passed
- *** TG 7 channel 25 on Slot 0 passed
- *** TG 7 channel 26 on Slot 0 passed
- *** TG 7 channel 27 on Slot 0 passed
- *** TG 8 channel 28 on Slot 0 passed
- *** TG 8 channel 29 on Slot 0 passed
- *** TG 8 channel 30 on Slot 0 passed
- *** TG 8 channel 31 on Slot 0 passed
- *** TG 9 channel 32 on Slot 0 passed
- *** TG 9 channel 33 on Slot 0 passed
- *** TG 9 channel 34 on Slot 0 passed
- *** TG 9 channel 35 on Slot 0 passed
- *** TG 10 channel 36 on Slot 0 passed
- *** TG 10 channel 37 on Slot 0 passed
- *** TG 10 channel 38 on Slot 0 passed
- *** TG 10 channel 39 on Slot 0 passed
- *** TG 11 channel 40 on Slot 0 passed
- *** TG 11 channel 41 on Slot 0 passed
- *** TG 11 channel 42 on Slot 0 passed
- *** TG 11 channel 43 on Slot 0 passed
- *** TG 12 channel 44 on Slot 0 passed
- *** TG 12 channel 45 on Slot 0 passed
- *** TG 12 channel 46 on Slot 0 passed
- *** TG 12 channel 47 on Slot 0 passed
- *** TG 13 channel 48 on Slot 0 passed
- *** TG 13 channel 49 on Slot 0 passed
- *** TG 13 channel 50 on Slot 0 passed
- *** TG 13 channel 51 on Slot 0 passed
- *** TG 14 channel 52 on Slot 0 passed
- *** TG 14 channel 53 on Slot 0 passed
- *** TG 14 channel 54 on Slot 0 passed
- *** TG 14 channel 55 on Slot 0 passed
- *** TG 15 channel 56 on Slot 0 passed
- *** TG 15 channel 57 on Slot 0 passed
- *** TG 15 channel 58 on Slot 0 passed
- *** TG 15 channel 59 on Slot 0 passed
- *** TG 16 channel 60 on Slot 0 passed
- *** TG 16 channel 61 on Slot 0 passed
- *** TG 16 channel 62 on Slot 0 passed
- *** TG 16 channel 63 on Slot 0 passed
- Starting Dilbert register tests
- *** DILBERT FPGA Revision on slot 0 is: 12
- *** DILBERT Register Test on Slot 0 passed
- Starting Pequot register tests
- *** PEQUOT channel 0 on Slot 0 passed
- *** PEQUOT channel 1 on Slot 0 passed
- *** PEQUOT channel 2 on Slot 0 passed
- *** PEQUOT channel 3 on Slot 0 passed

- *** PEQUOT channel 4 on Slot 0 passed
- *** PEQUOT channel 5 on Slot 0 passed
- *** PEQUOT channel 6 on Slot 0 passed
- *** PEQUOT channel 7 on Slot 0 passed
- *** PEQUOT channel 8 on Slot 0 passed
- *** PEQUOT channel 9 on Slot 0 passed
- *** PEQUOT channel 10 on Slot 0 passed
- *** PEQUOT channel 11 on Slot 0 passed
- *** PEQUOT channel 12 on Slot 0 passed
- *** PEQUOT channel 13 on Slot 0 passed
- *** PEQUOT channel 14 on Slot 0 passed
- *** PEQUOT channel 15 on Slot 0 passed
- *** PEQUOT channel 16 on Slot 0 passed
- *** PEQUOT channel 17 on Slot 0 passed
- *** PEQUOT channel 18 on Slot 0 passed
- *** PEQUOT channel 19 on Slot 0 passed
- *** PEQUOT channel 20 on Slot 0 passed
- *** PEQUOT channel 21 on Slot 0 passed
- *** PEQUOT channel 22 on Slot 0 passed
- *** PEQUOT channel 23 on Slot 0 passed
- *** PEQUOT channel 24 on Slot 0 passed
- *** PEQUOT channel 25 on Slot 0 passed
- *** PEQUOT channel 26 on Slot 0 passed
- *** PEQUOT channel 27 on Slot 0 passed
- *** PEQUOT channel 28 on Slot 0 passed
- *** PEQUOT channel 29 on Slot 0 passed
- *** PEQUOT channel 30 on Slot 0 passed
- *** PEQUOT channel 31 on Slot 0 passed
- *** PEQUOT channel 32 on Slot 0 passed
- *** PEQUOT channel 33 on Slot 0 passed
- *** PEQUOT channel 34 on Slot 0 passed
- *** PEQUOT channel 35 on Slot 0 passed
- *** PEQUOT channel 36 on Slot 0 passed
- *** PEQUOT channel 37 on Slot 0 passed
- *** PEQUOT channel 38 on Slot 0 passed
- *** PEQUOT channel 39 on Slot 0 passed
- *** PEQUOT channel 40 on Slot 0 passed
- *** PEQUOT channel 41 on Slot 0 passed
- *** PEQUOT channel 42 on Slot 0 passed
- *** PEQUOT channel 43 on Slot 0 passed
- *** PEQUOT channel 44 on Slot 0 passed
- *** PEQUOT channel 45 on Slot 0 passed
- *** PEQUOT channel 46 on Slot 0 passed
- *** PEQUOT channel 47 on Slot 0 passed
- *** PEQUOT channel 48 on Slot 0 passed
- *** PEQUOT channel 49 on Slot 0 passed
- *** PEQUOT channel 50 on Slot 0 passed
- *** PEQUOT channel 51 on Slot 0 passed
- *** PEQUOT channel 52 on Slot 0 passed
- *** PEQUOT channel 53 on Slot 0 passed
- *** PEQUOT channel 54 on Slot 0 passed
- *** PEQUOT channel 55 on Slot 0 passed

- *** PEQUOT channel 56 on Slot 0 passed
- *** PEQUOT channel 57 on Slot 0 passed
- *** PEQUOT channel 58 on Slot 0 passed
- *** PEQUOT channel 59 on Slot 0 passed
- *** PEQUOT channel 60 on Slot 0 passed
- *** PEQUOT channel 61 on Slot 0 passed
- *** PEQUOT channel 62 on Slot 0 passed
- *** PEQUOT channel 63 on Slot 0 passed
- Testing slot 1
- Starting PG register tests
- *** PG Register Tests on Slot 1 passed
- Starting TG register tests
- *** TG 1 channel 0 on Slot 1 passed
- *** TG 1 channel 1 on Slot 1 passed
- *** TG 1 channel 2 on Slot 1 passed
- *** TG 1 channel 3 on Slot 1 passed
- *** TG 2 channel 4 on Slot 1 passed
- *** TG 2 channel 5 on Slot 1 passed
- *** TG 2 channel 6 on Slot 1 passed
- *** TG 2 channel 7 on Slot 1 passed
- *** TG 3 channel 8 on Slot 1 passed
- *** TG 3 channel 9 on Slot 1 passed
- *** TG 3 channel 10 on Slot 1 passed
- *** TG 3 channel 11 on Slot 1 passed
- *** TG 4 channel 12 on Slot 1 passed
- *** TG 4 channel 13 on Slot 1 passed
- *** TG 4 channel 14 on Slot 1 passed
- *** TG 4 channel 15 on Slot 1 passed
- *** TG 5 channel 16 on Slot 1 passed
- *** TG 5 channel 17 on Slot 1 passed
- *** TG 5 channel 18 on Slot 1 passed
- *** TG 5 channel 19 on Slot 1 passed
- *** TG 6 channel 20 on Slot 1 passed
- *** TG 6 channel 21 on Slot 1 passed
- *** TG 6 channel 22 on Slot 1 passed
- *** TG 6 channel 23 on Slot 1 passed
- *** TG 7 channel 24 on Slot 1 passed
- *** TG 7 channel 25 on Slot 1 passed
- *** TG 7 channel 26 on Slot 1 passed
- *** TG 7 channel 27 on Slot 1 passed
- *** TG 8 channel 28 on Slot 1 passed
- *** TG 8 channel 29 on Slot 1 passed
- *** TG 8 channel 30 on Slot 1 passed
- *** TG 8 channel 31 on Slot 1 passed
- *** TG 9 channel 32 on Slot 1 passed
- *** TG 9 channel 33 on Slot 1 passed
- *** TG 9 channel 34 on Slot 1 passed
- *** TG 9 channel 35 on Slot 1 passed
- *** TG 10 channel 36 on Slot 1 passed
- *** TG 10 channel 37 on Slot 1 passed
- *** TG 10 channel 38 on Slot 1 passed
- *** TG 10 channel 39 on Slot 1 passed

- *** TG 11 channel 40 on Slot 1 passed
- *** TG 11 channel 41 on Slot 1 passed
- *** TG 11 channel 42 on Slot 1 passed
- *** TG 11 channel 43 on Slot 1 passed
- *** TG 12 channel 44 on Slot 1 passed
- *** TG 12 channel 45 on Slot 1 passed
- *** TG 12 channel 46 on Slot 1 passed
- *** TG 12 channel 47 on Slot 1 passed
- *** TG 13 channel 48 on Slot 1 passed
- *** TG 13 channel 49 on Slot 1 passed
- *** TG 13 channel 50 on Slot 1 passed
- *** TG 13 channel 51 on Slot 1 passed
- *** TG 14 channel 52 on Slot 1 passed
- *** TG 14 channel 53 on Slot 1 passed
- *** TG 14 channel 54 on Slot 1 passed
- *** TG 14 channel 55 on Slot 1 passed
- *** TG 15 channel 56 on Slot 1 passed
- *** TG 15 channel 57 on Slot 1 passed
- *** TG 15 channel 58 on Slot 1 passed
- *** TG 15 channel 59 on Slot 1 passed
- *** TG 16 channel 60 on Slot 1 passed
- *** TG 16 channel 61 on Slot 1 passed
- *** TG 16 channel 62 on Slot 1 passed
- *** TG 16 channel 63 on Slot 1 passed
- Starting Dilbert register tests
- *** DILBERT FPGA Revision on slot 1 is: 12
- *** DILBERT Register Test on Slot 1 passed
- Starting Pequot register tests
- *** PEQUOT channel 0 on Slot 1 passed
- *** PEQUOT channel 1 on Slot 1 passed
- *** PEQUOT channel 2 on Slot 1 passed
- *** PEQUOT channel 3 on Slot 1 passed
- *** PEQUOT channel 4 on Slot 1 passed
- *** PEQUOT channel 5 on Slot 1 passed
- *** PEQUOT channel 6 on Slot 1 passed
- *** PEQUOT channel 7 on Slot 1 passed
- *** PEQUOT channel 8 on Slot 1 passed
- *** PEQUOT channel 9 on Slot 1 passed
- *** PEQUOT channel 10 on Slot 1 passed
- *** PEQUOT channel 11 on Slot 1 passed
- *** PEQUOT channel 12 on Slot 1 passed
- *** PEQUOT channel 13 on Slot 1 passed
- *** PEQUOT channel 14 on Slot 1 passed
- *** PEQUOT channel 15 on Slot 1 passed
- *** PEQUOT channel 16 on Slot 1 passed
- *** PEQUOT channel 17 on Slot 1 passed
- *** PEQUOT channel 18 on Slot 1 passed
- *** PEQUOT channel 19 on Slot 1 passed
- *** PEQUOT channel 20 on Slot 1 passed
- *** PEQUOT channel 21 on Slot 1 passed
- *** PEQUOT channel 22 on Slot 1 passed
- *** PEQUOT channel 23 on Slot 1 passed

- *** PEQUOT channel 24 on Slot 1 passed
- *** PEQUOT channel 25 on Slot 1 passed
- *** PEQUOT channel 26 on Slot 1 passed
- *** PEQUOT channel 27 on Slot 1 passed
- *** PEQUOT channel 28 on Slot 1 passed
- *** PEQUOT channel 29 on Slot 1 passed
- *** PEQUOT channel 30 on Slot 1 passed
- *** PEQUOT channel 31 on Slot 1 passed
- *** PEQUOT channel 32 on Slot 1 passed
- *** PEQUOT channel 33 on Slot 1 passed
- *** PEQUOT channel 34 on Slot 1 passed
- *** PEQUOT channel 35 on Slot 1 passed
- *** PEQUOT channel 36 on Slot 1 passed
- *** PEQUOT channel 37 on Slot 1 passed
- *** PEQUOT channel 38 on Slot 1 passed
- *** PEQUOT channel 39 on Slot 1 passed
- *** PEQUOT channel 40 on Slot 1 passed
- *** PEQUOT channel 41 on Slot 1 passed
- *** PEQUOT channel 42 on Slot 1 passed
- *** PEQUOT channel 43 on Slot 1 passed
- *** PEQUOT channel 44 on Slot 1 passed
- *** PEQUOT channel 45 on Slot 1 passed
- *** PEQUOT channel 46 on Slot 1 passed
- *** PEQUOT channel 47 on Slot 1 passed
- *** PEQUOT channel 48 on Slot 1 passed
- *** PEQUOT channel 49 on Slot 1 passed
- *** PEQUOT channel 50 on Slot 1 passed
- *** PEQUOT channel 51 on Slot 1 passed
- *** PEQUOT channel 52 on Slot 1 passed
- *** PEQUOT channel 53 on Slot 1 passed
- *** PEQUOT channel 54 on Slot 1 passed
- *** PEQUOT channel 55 on Slot 1 passed
- *** PEQUOT channel 56 on Slot 1 passed
- *** PEQUOT channel 57 on Slot 1 passed
- *** PEQUOT channel 58 on Slot 1 passed
- *** PEQUOT channel 59 on Slot 1 passed
- *** PEQUOT channel 60 on Slot 1 passed
- *** PEQUOT channel 61 on Slot 1 passed
- *** PEQUOT channel 62 on Slot 1 passed
- *** PEQUOT channel 63 on Slot 1 passed
- Finished CB200 Register Tests on all slots
- Beginning JTAG Bus Control
- *** JTAG Bus Controller Rev. on slot 0 is: 8
- JTAG Bus Control Port 0 - TDI Word 5 slot 0 passed
- DSMTO Rider Card Not Present on slot 0 - Port 1 Skipped
- *** JTAG Bus Controller Rev. on slot 1 is: 8
- JTAG Bus Control Port 0 - TDI Word 5 slot 1 passed
- DSMTO Rider Card Not Present on slot 1 - Port 1 Skipped
- Finished JTAG Bus Control on all slots
- Beginning PG LVM Short BIST test
- Finished on all slots
- Beginning TG LVM Short BIST test

- Finished on all slots
- Beginning PG Opcode test
- Beginning Basic PG Opcodes test
  - Beginning Halt Opcode test
  - Beginning Repeat Opcode, Minimum Value test
  - Beginning Repeat Opcode, Maximum Value test
  - Beginning Repeat Opcode test
  - Beginning Change Repeat Opcode from the test program test
  - Beginning Jump Opcode test
- Completed Basic PG Opcodes test
- Beginning Condition Flags PG Opcodes test
  - Beginning burst_clear_flags test
  - Beginning burst_setA test
  - Beginning burst_enableA test
  - Beginning burst_clearA test
  - Beginning burst_setB test
  - Beginning burst_enableB test
  - Beginning burst_clearB test
  - Beginning burst_setC test
  - Beginning burst_enableC test
  - Beginning burst_clearC test
  - Beginning burst_setD test
  - Beginning burst_enableD test
  - Beginning burst_clearD test
- Beginning Jump PG Opcodes test
  - Beginning burst_jmp test
  - Beginning burst_nestjmp test
  - Beginning burst_fnestjmp test
  - Beginning burst_cndjmp test
  - Beginning burst_negcndjmp test
  - Beginning burst_clrcnd1jmp test
  - Beginning burst_clrcnd2jmp test
  - Beginning burst_glo_nstjmp test
  - Beginning burst_glo_cndjmp test
  - Beginning burst_glo_clrcndjmp test
- Beginning Call PG Opcodes test
  - Beginning burst_call test
  - Beginning burst_nestcall test
  - Beginning burst_fnestcall test
  - Beginning burst_cndcall test
  - Beginning burst_negcndcall test
  - Beginning burst_clrcnd1call test
  - Beginning burst_clrcnd2call test
  - Beginning burst_glo_call test
  - Beginning burst_glo_cndcall test
  - Beginning burst_glo_clrcndcall test
  - Beginning burst_ccall test
  - Beginning burst_ccall test
  - Beginning burst_glo_clrcndjmp test
- Beginning Return PG Opcodes test
  - Beginning burst_nestrtn test
  - Beginning burst_cndrtn test

- Beginning burst_ncndrtn test
- Beginning burst_cndrtnclr test
- Beginning burst_glo_callrtn test
- Beginning Resume PG Opcodes test
- Beginning burst_resume test
- Beginning burst_cndresume test
- Beginning burst_cndresumeclr test
- Beginning Push & Pop PG Opcodes test
- Beginning burst_pushpop test
- Beginning burst_nstpushpop test
- Beginning burst_ovfpushpop test
- Beginning Loop PG Opcodes test
- Beginning burst_setloop test
- Beginning burst_loop test
- Beginning burst_maxloopA test
- Beginning burst_maxloopB test
- Beginning burst_maxloopC test
- Beginning burst_nstpushpop test
- Beginning burst_nestloop test
- Beginning burst_nestloop1 test
- Beginning burst_nestloop2 test
- Beginning burst_nestloop3 test
- Beginning burst_useloopB test
- Beginning burst_useloopC test
- Beginning burst_loop_init test
- Beginning burst_poploop test
- Beginning burst_nstpoploop test
- Beginning Exit Loop PG Opcodes test
- Beginning burst_exitloop test
- Beginning burst_cndexit test
- Beginning burst_ncndexit test
- Beginning burst_cndexitclr test
- Beginning burst_one Pat Gen, set_code
- Beginning Pat Gen, tl_PatgenClrCode
- Beginning burst_AAAA Pat Gen, set_code
- Beginning Pat Gen, clr_code
- Beginning burst_5555 Pat Gen, set_code
- Beginning Pat Gen, clr_code
- Beginning burst_zero Pat Gen, set_code
- Beginning Misc PG Opcodes test
- Beginning Halt End Module
- Beginning NOP End Module
- Beginning Fail Count
- Beginning Clear Fail
- Beginning Inhibit Fail Count
- Beginning Inhibit Cycle Count
- Beginning Mask
- Beginning Halt on Failure
- Beginning IGN Control Bit
- Beginning STV
- Beginning Basic PG Opcodes test
- Beginning Halt Opcode test

- Beginning Repeat Opcode, Minimum Value test
- Beginning Repeat Opcode, Maximum Value test
- Beginning Repeat Opcode test
- Beginning Change Repeat Opcode from the test program test
- Beginning Jump Opcode test
- Completed Basic PG Opcodes test
- Beginning Condition Flags PG Opcodes test
- Beginning burst_clear_flags test
- Beginning burst_setA test
- Beginning burst_enableA test
- Beginning burst_clearA test
- Beginning burst_setB test
- Beginning burst_enableB test
- Beginning burst_clearB test
- Beginning burst_setC test
- Beginning burst_enableC test
- Beginning burst_clearC test
- Beginning burst_setD test
- Beginning burst_enableD test
- Beginning burst_clearD test
- Beginning Jump PG Opcodes test
- Beginning burst_jmp test
- Beginning burst_nestjmp test
- Beginning burst_fnestjmp test
- Beginning burst_cndjmp test
- Beginning burst_negcndjmp test
- Beginning burst_clrcnd1jmp test
- Beginning burst_clrcnd2jmp test
- Beginning burst_glo_nstjmp test
- Beginning burst_glo_cndjmp test
- Beginning burst_glo_clrcndjmp test
- Beginning Call PG Opcodes test
- Beginning burst_call test
- Beginning burst_nestcall test
- Beginning burst_fnestcall test
- Beginning burst_cndcall test
- Beginning burst_negcndcall test
- Beginning burst_clrcnd1call test
- Beginning burst_clrcnd2call test
- Beginning burst_glo_call test
- Beginning burst_glo_cndcall test
- Beginning burst_glo_clrcndcall test
- Beginning burst_ccall test
- Beginning burst_ccall test
- Beginning burst_glo_clrcndjmp test
- Beginning Return PG Opcodes test
- Beginning burst_nestrtn test
- Beginning burst_cndrtn test
- Beginning burst_ncndrtn test
- Beginning burst_cndrtnclr test
- Beginning burst_glo_callrtn test
- Beginning Resume PG Opcodes test

- Beginning burst_resume test
- Beginning burst_cndresume test
- Beginning burst_cndresumeclr test
- Beginning Push & Pop PG Opcodes test
- Beginning burst_pushpop test
- Beginning burst_nstpushpop test
- Beginning burst_ovfpushpop test
- Beginning Loop PG Opcodes test
- Beginning burst_setloop test
- Beginning burst_loop test
- Beginning burst_maxloopA test
- Beginning burst_maxloopB test
- Beginning burst_maxloopC test
- Beginning burst_nstpushpop test
- Beginning burst_nestloop test
- Beginning burst_nestloop1 test
- Beginning burst_nestloop2 test
- Beginning burst_nestloop3 test
- Beginning burst_useloopB test
- Beginning burst_useloopC test
- Beginning burst_loop_init test
- Beginning burst_poploop test
- Beginning burst_nstpoploop test
- Beginning Exit Loop PG Opcodes test
- Beginning burst_exitloop test
- Beginning burst_cndexit test
- Beginning burst_ncndexit test
- Beginning burst_cndexitclr test
- Beginning burst_one Pat Gen, set_code
- Beginning Pat Gen, tl_PatgenClrCode
- Beginning burst_AAAA Pat Gen, set_code
- Beginning Pat Gen, clr_code
- Beginning burst_5555 Pat Gen, set_code
- Beginning Pat Gen, clr_code
- Beginning burst_zero Pat Gen, set_code
- Beginning Misc PG Opcodes test
- Beginning Halt End Module
- Beginning NOP End Module
- Beginning Fail Count
- Beginning Clear Fail
- Beginning Inhibit Fail Count
- Beginning Inhibit Cycle Count
- Beginning Mask
- Beginning Halt on Failure
- Beginning IGN Control Bit
- Beginning STV
- Finished on all slots
- Beginning StateBus Test test
- Statebus : Checking STB lines : Dual mode, 30MHz
- Statebus : Checking STB lines : Dual mode, 50MHz
- Statebus : Checking STB lines : Dual mode, 80MHz
- Statebus : Checking STB lines : Dual mode, 100MHz

- Statebus : Checking STB lines : Quad mode, 30MHz
- Statebus : Checking STB lines : Quad mode, 50MHz
- Statebus : Checking STB lines : Quad mode, 80MHz
- Statebus : Checking STB lines : Quad mode, 100MHz
- Statebus : Checking STB lines : Quad mode, 200MHz
- Statebus : Checking State number lines : Single mode, 25MHz
- Statebus : Checking State number lines : Single mode, 30MHz
- Statebus : Checking State number lines : Single mode, 50MHz
- Statebus : Checking State number lines : Quad mode, 50MHz
- Statebus : Checking State number lines : Quad mode, 100MHz
- Statebus : Checking State number lines : Quad mode, 150MHz
- Statebus : Checking State number lines : Quad mode, 200MHz
- Statebus : Checking ADSS, MASK, CFAIL, FmtFAIL : Single mode, 25MHz
- Statebus : Checking ADSS, MASK, CFAIL, FmtFAIL : Single mode, 30MHz
- Statebus : Checking ADSS, MASK, CFAIL, FmtFAIL : Single mode, 35MHz
- Statebus : Checking ADSS, MASK, CFAIL, FmtFAIL : Single mode, 50MHz
- Statebus : Checking ADSS, MASK, CFAIL, FmtFAIL : Dual mode, 35MHz
- Statebus : Checking ADSS, MASK, CFAIL, FmtFAIL : Dual mode, 50MHz
- Statebus : Checking ADSS, MASK, CFAIL, FmtFAIL : Dual mode, 80MHz
- Statebus : Checking ADSS, MASK, CFAIL, FmtFAIL : Dual mode, 100MHz
- Statebus : Checking ADSS, MASK, CFAIL, FmtFAIL : Quad mode, 50MHz
- Statebus : Checking ADSS, MASK, CFAIL, FmtFAIL : Quad mode, 100MHz
- Statebus : Checking ADSS, MASK, CFAIL, FmtFAIL : Quad mode, 150MHz
- Statebus : Checking ADSS, MASK, CFAIL, FmtFAIL : Quad mode, 200MHz
- Statebus : Checking STB lines : Dual mode, 30MHz
- Statebus : Checking STB lines : Dual mode, 50MHz
- Statebus : Checking STB lines : Dual mode, 80MHz
- Statebus : Checking STB lines : Dual mode, 100MHz
- Statebus : Checking STB lines : Quad mode, 30MHz
- Statebus : Checking STB lines : Quad mode, 50MHz
- Statebus : Checking STB lines : Quad mode, 80MHz
- Statebus : Checking STB lines : Quad mode, 100MHz
- Statebus : Checking STB lines : Quad mode, 200MHz
- Statebus : Checking State number lines : Single mode, 25MHz
- Statebus : Checking State number lines : Single mode, 30MHz
- Statebus : Checking State number lines : Single mode, 50MHz
- Statebus : Checking State number lines : Quad mode, 50MHz
- Statebus : Checking State number lines : Quad mode, 100MHz
- Statebus : Checking State number lines : Quad mode, 150MHz
- Statebus : Checking State number lines : Quad mode, 200MHz
- Statebus : Checking ADSS, MASK, CFAIL, FmtFAIL : Single mode, 25MHz
- Statebus : Checking ADSS, MASK, CFAIL, FmtFAIL : Single mode, 30MHz
- Statebus : Checking ADSS, MASK, CFAIL, FmtFAIL : Single mode, 35MHz
- Statebus : Checking ADSS, MASK, CFAIL, FmtFAIL : Single mode, 50MHz
- Statebus : Checking ADSS, MASK, CFAIL, FmtFAIL : Dual mode, 35MHz
- Statebus : Checking ADSS, MASK, CFAIL, FmtFAIL : Dual mode, 50MHz
- Statebus : Checking ADSS, MASK, CFAIL, FmtFAIL : Dual mode, 80MHz
- Statebus : Checking ADSS, MASK, CFAIL, FmtFAIL : Dual mode, 100MHz
- Statebus : Checking ADSS, MASK, CFAIL, FmtFAIL : Quad mode, 50MHz
- Statebus : Checking ADSS, MASK, CFAIL, FmtFAIL : Quad mode, 100MHz
- Statebus : Checking ADSS, MASK, CFAIL, FmtFAIL : Quad mode, 150MHz
- Statebus : Checking ADSS, MASK, CFAIL, FmtFAIL : Quad mode, 200MHz

- Finished StateBus Test on all slots
- Beginning StateBus Tset
- ...Testing Slot# 0 Tset Bit 0 <-> Tset# 1
- ...Testing Slot# 0 Tset Bit 1 <-> Tset# 2
- ...Testing Slot# 0 Tset Bit 2 <-> Tset# 4
- ...Testing Slot# 0 Tset Bit 3 <-> Tset# 8
- ...Testing Slot# 0 Tset Bit 4 <-> Tset# 16
- ...Testing Slot# 0 Tset Bit 5 <-> Tset# 32
- ...Testing Slot# 0 Tset Bit 6 <-> Tset# 64
- ...Testing Slot# 1 Tset Bit 0 <-> Tset# 1
- ...Testing Slot# 1 Tset Bit 1 <-> Tset# 2
- ...Testing Slot# 1 Tset Bit 2 <-> Tset# 4
- ...Testing Slot# 1 Tset Bit 3 <-> Tset# 8
- ...Testing Slot# 1 Tset Bit 4 <-> Tset# 16
- ...Testing Slot# 1 Tset Bit 5 <-> Tset# 32
- ...Testing Slot# 1 Tset Bit 6 <-> Tset# 64
- Finished StateBus Tset on all slots
- Beginning HRAM test
- HRAM Trigger tests
- HRAM Control - Checking triggering: trig cond - 1st parameter
- Testing Trigger On First Vector
- Testing Trigger On Fail Vector
- Testing Trigger on STV
- HRAM Control - Checking triggering: wait for event - 2nd parameter
- Testing Trigger On First Vector
- Testing Wait For Event
- HRAM Control - Checking triggering: Pretrig - 3rd parameter
- HRAM Control - Checking triggering: stops on full - 4th parameter
- HRAM Control - Checking capture
- Testing Capture All
- Testing Capture Fail
- Testing Capture STV
- Testing Capture Fail STV
- Testing Compress Repeats
- HRAM Override tests
- HRAM Control - Checking KeepAlive Override
- HRAM Control - Checking Priming & Flushing Override
- HRAM Control - Checking Repeat Override
- HRAM Trigger tests
- HRAM Control - Checking triggering: trig cond - 1st parameter
- Testing Trigger On First Vector
- Testing Trigger On Fail Vector
- Testing Trigger on STV
- HRAM Control - Checking triggering: wait for event - 2nd parameter
- Testing Trigger On First Vector
- Testing Wait For Event
- HRAM Control - Checking triggering: Pretrig - 3rd parameter
- HRAM Control - Checking triggering: stops on full - 4th parameter
- HRAM Control - Checking capture
- Testing Capture All
- Testing Capture Fail
- Testing Capture STV

- Testing Capture Fail STV
- Testing Compress Repeats
- HRAM Override tests
- HRAM Control - Checking KeepAlive Override
- HRAM Control - Checking Priming & Flushing Override
- HRAM Control - Checking Repeat Override
- Finished on HRAM Tests all slots
- Beginning Drive Compare Formats test
- Starting StartState OFF Tests, Single Mode
- Starting StartState NONE Tests, Single Mode
- Starting StartState FMT Tests, Single Mode
- Starting StartState HI/LO Tests, Single Mode
- Starting 40/60 Window Tests, Single Mode
- Starting 40/90 Window Tests, Single Mode
- Starting 20/60 Window Tests, Single Mode
- Starting Compare Valid Tests, Single Mode
- Starting Compare Midband Tests, Single Mode
- Starting Compare Hi Tests, Single Mode
- Starting Compare Low Tests, Single Mode
- Starting Compare Mask Tests, Single Mode
- Starting Compare Valid Tests, Dual Mode
- Starting Compare Midband Tests, Dual Mode
- Starting Compare Hi Tests, Dual Mode
- Starting Compare Low Tests, Dual Mode
- Starting Compare Mask Tests, Dual Mode
- Starting Compare Valid Tests, Quad Mode
- Starting Compare Midband Tests, Quad Mode
- Starting Compare Hi Tests, Quad Mode
- Starting Compare Low Tests, Quad Mode
- Starting Compare Mask Tests, Quad Mode
- Finished Drive Compare Formats Test on all slots
- Beginning Drive Compare Formats test
- Checking drive formats in single mode
- Checking drive formats in dual mode
- Checking drive formats in quad mode
- Finished on all slots
- Beginning Drive Compare Levels test
    - Beginning Vih Test with level set to: 1.5 Volts
    - Beginning Vih Test with level set to: 3 Volts
    - Beginning Vih Test with level set to: 4.5 Volts
    - Beginning Vih Test with level set to: 5.75 Volts
    - Beginning Vil Test with level set to: -0.75 Volts
    - Beginning Vil Test with level set to: 0.5 Volts
    - Beginning Vil Test with level set to: 2 Volts
    - Beginning Vil Test with level set to: 3.5 Volts
    - Beginning Voh Test with level set to: +3.5 Volts
    - Beginning Voh Test with level set to: +4.5 Volts
    - Beginning Voh Test with level set to: +5.5 Volts
    - Beginning Vol Test with level set to: +1.5 Volts
    - Beginning Vol Test with level set to: +0.5 Volts
    - Beginning Vol Test with level set to: -0.5 Volts.
- Finished Drive Compare Levels on all slots

- Beginning Levels Memory BIST
- Actual BIST Time for All boards = 0.15625secs
- Levels Memory BIST Passed on Slot: 0
- Levels Memory BIST Passed on Slot: 1
- Finished Levels Memory BIST on all slots
- Completed Channel_Board test on slot 1

%JOB_END - ****PASSED**** Channel_Board Quick Check of slot(s) 0, 1 at 12:03:10 PM
- PASS slot 0 (S/N XXX)
- PASS slot 1 (S/N XXX)

%JOB_START - Beginning DPS Quick Check test on slot 22 at 12:03:23 PM on 1/17/2020
Workbook Rev V7.60.40IP02 DC1116 IG-XL Version: 3.50.40IP02 DIB: P/N 51745600 S/N xxx Rev 0901A

%INFO - ----------
%INFO - System IP750_xxxE (IP750EX)
%INFO - IG-XL 3.50.40IP02, Build: 04.13.11.20.00
%INFO - Maintenance 7.60.40IP02, Build: 04.18.11.02.09
%INFO - ----------
- Verifying DPS Current Leakage
- Channel 0
- Channel 1
- Channel 2
- Channel 3
- Channel 4
- Channel 5
- Channel 6
- Channel 7
- Finished Verifying DPS Current Leakage

%JOB_END - ****PASSED**** DPS Quick Check of slot 22 (S/N:CXXXXX) at 12:03:26 PM

%JOB_START - Beginning ICUA Quick Check test on slot 2 at 12:03:38 PM on 1/17/2020
Workbook Rev V7.60.40IP02 DC1116 IG-XL Version: 3.50.40IP02 DIB: P/N 51745600 S/N xxx Rev 0901A

%INFO - ----------
%INFO - System IP750_xxxE (IP750EX)
%INFO - IG-XL 3.50.40IP02, Build: 04.13.11.20.00
%INFO - Maintenance 7.60.40IP02, Build: 04.18.11.02.09
%INFO - ----------
- ICUA-2 P/N:51742601 Rev:738B S/N:XXXX
- %INFO -- ADM on ICUA-2 Chan0 Slot2, ADM P/N:51740520 Rev:735C S/N:
- %INFO -- ADM on ICUA-2 Chan1 Slot2, ADM P/N:51740520 Rev:735C S/N:40
- %INFO -- ADM on ICUA-2 Chan2 Slot2, ADM P/N:51740520 Rev:735C S/N:4
- %INFO -- ADM on ICUA-2 Chan3 Slot2, ADM P/N:51740520 Rev:735C S/N:40
- ICUA-2 Relay board P/N:51742800 Rev:515C S/N:4

- *** Start to test on Multi PC Environment ***
- [Check the existence of Giga-Channel on PCs]

- ImagePC#0
- [Overlap Check Giga-Channel NodeID on Image Processing PC]

- -- Check on Token Link Connection
- Starting PG_History_Ram
- Completed PG_History_Ram
- Starting PG_Svm_Ram
- Completed PG_Svm_Ram
- Starting PG_Scramble_Ram, ADSS
- Completed PG_Scramble_Ram
- Starting PG_Scramble_Ram, Tset
- Completed PG_Scramble_Ram
- Starting PG_LVM_BIST_Ram (up to 32 sec)
- Completed PG_LVM_BIST_Ram in 21.6 sec

- %INFO - LRS Off
- Starting TG Register Tests...
- Completed TG Register Tests
- Starting ICUA_TG_Period_Ram...
- Completed ICUA_TG_Period_Ram
- Starting ICUA_TG_Period_Map_Ram...
- Completed TG_Period_Map_Ram
- Starting TG_LVM_BIST_Ram (up to 32 sec)
- Completed TG_LVM_BIST_Ram in 10.8 sec
- Starting ICUA_TG_History_Ram
- Completed ICUA_TG_History_Ram
- Starting ICUA_TG_SVM_Ram
- Completed ICUA_TG_SVM_Ram
- Starting ICUA_TG_ADSS_Ram
- Completed ICUA_TG_ADSS_Ram
- Starting ICUA_TG_KeepAlive_Ram
- Completed ICUA_TG_KeepAlive_Ram
- Starting ICUA_TG_Tset_LkDwn_Ram
- Completed ICUA_TG_Tset_LkDwn_Ram
- Starting ICUA_TG_Edge_Ram
- Completed ICUA_TG_Edge_Ram
- Starting ICUA_TG_Format_Ram
- Completed ICUA_TG_Format_Ram
- Starting ICUA_TG_FormatLkDwn_Ram
- Completed ICUA_TG_FormatLkDwn_Ram
- %INFO - LRS On

- Starting ICUA MEM & MOV FPGA Registers...
- [ICUA Global IDL Register Check]
- [ICUA Channel Select IDL Register Check - Chan0]
- [Data Transfer and Giga Channel Control Register Check - Chan0]
- [ICUA Channel Select IDL Register Check - Chan1]
- [Data Transfer and Giga Channel Control Register Check - Chan1]
- [ICUA Channel Select IDL Register Check - Chan2]
- [Data Transfer and Giga Channel Control Register Check - Chan2]
- [ICUA Channel Select IDL Register Check - Chan3]
- [Data Transfer and Giga Channel Control Register Check - Chan3]

- [Data Transfer and Giga Channel Control Register Check]
- Completed ICUA MEM & MOV FPGA Registers

- Starting PPMU FPGA Registers
- Completed PPMU FPGA Registers

- Start Thermosensor Check...
- Completed Thermosensor Check

- Start ICUA board SDRAM/SVM Quick Check
- Start ICUA SDRAM Check...
- [Data Uniqueness Test]
- [Address Uniqueness Test]
- [Data Dump Test(1K)]
- Completed ICUA SDRAM Check
- Start ICUA SVM Check...
- [Data Uniqueness Test]
- [Address Uniqueness Test]
- [Data Dump Test(1K)]
- Completed ICUA SVM Check
- Completed ICUA board SDRAM/SVM Quick check

- Start ICUA board Download check...
- [1k words Download check]
- [Download SDRAM source address uniqueness check]
- [Download SVM destination address uniqueness check]
- [Up to 1k words Download check]
- Completed ICUA board Download check

- Start ICUA_ADC_DAC Check...
- [A/D Converter Ground Source Measure Test]
- [RefDAC Voltage Test Measured by ADC on ICUA]
- [PPMU DAC Voltage Test Measured by ADC on ICUA]
- Completed ICUA_ADC_DAC Check

- Start ICUA Utility Bit Check...
- Completed ICUA Utility Bit Check

- Starting State Bus test
- Statebus : Checking STB lines : Normal mode, 30MHz
- Statebus : Checking STB lines : Normal mode, 50MHz
- Statebus : Checking STB lines : Normal mode, 80MHz
- Statebus : Checking STB lines : Normal mode, 100MHz
- Statebus : Checking State number lines : Extended mode, 25MHz
- Statebus : Checking State number lines : Extended mode, 30MHz
- Statebus : Checking State number lines : Extended mode, 50MHz
- Completed State Bus test

- Start Capture Test [Checker Mode]...
- [Capture Test]
- [Capture Test(All Channel Capture)]
- [Accumulate Test]

- Completed Capture Test [Checker Mode]

- Start ADM Quick Check...
- [Check ADM at ICUA Chan 0]
- [ADM Power Supply Voltage Check]
- [ADM Capture Bank check]
- [Offset Adjust check] (ADM 50M-A/D Converter Capture)
- [Offset Adjust check] (ADM 25M-A/D Converter Capture)
- [Input Voltage Range Test]
- [ADM Post-CDS Amp check]
- [ADM OffsetRemover Dac check]
- [ADM Optical Black Remover Dac check]
- [Differential Terminate Path Test]
- [Check ADM at ICUA Chan 1]
- [ADM Power Supply Voltage Check]
- [ADM Capture Bank check]
- [Offset Adjust check] (ADM 50M-A/D Converter Capture)
- [Offset Adjust check] (ADM 25M-A/D Converter Capture)
- [Input Voltage Range Test]
- [ADM Post-CDS Amp check]
- [ADM OffsetRemover Dac check]
- [ADM Optical Black Remover Dac check]
- [Differential Terminate Path Test]
- [Check ADM at ICUA Chan 2]
- [ADM Power Supply Voltage Check]
- [ADM Capture Bank check]
- [Offset Adjust check] (ADM 50M-A/D Converter Capture)
- [Offset Adjust check] (ADM 25M-A/D Converter Capture)
- [Input Voltage Range Test]
- [ADM Post-CDS Amp check]
- [ADM OffsetRemover Dac check]
- [ADM Optical Black Remover Dac check]
- [Differential Terminate Path Test]
- [Check ADM at ICUA Chan 3]
- [ADM Power Supply Voltage Check]
- [ADM Capture Bank check]
- [Offset Adjust check] (ADM 50M-A/D Converter Capture)
- [Offset Adjust check] (ADM 25M-A/D Converter Capture)
- [Input Voltage Range Test]
- [ADM Post-CDS Amp check]
- [ADM OffsetRemover Dac check]
- [ADM Optical Black Remover Dac check]
- [Differential Terminate Path Test]
- Completed ADM Quick Check

- == Running with Image Processing PC(IMGPC0) for Data Transfer Tests ==
- Start ICUA board Giga Channel data transfer check...
- [Acquire function check without averaging]
- 32-bit data transfer check
- [Acquire function check with averaging]
- -- 16bit GAIN bit check

- -- 24bit data divide check
- Completed ICUA board Giga Channel data transfer check

- Start APC-485T FIFO Check ...
- [Memory Size: 16777216 Bytes]
- Completed APC-485T FIFO Check

- Start APM-425T CheckSum Bit Check...
- 32-bit data transfer and all checksum bit check
- Completed APM-425T CheckSum Bit Check...

- Completed ICUA Quick Check 68.3 sec

%JOB_END - ****PASSED**** ICUA Quick Check of slot 2 (S/N:) at 12:04:46 PM

%JOB_START - Beginning APMU Quick Check test on slot 5 at 12:04:59 PM on 1/17/2020
Workbook Rev V7.60.40IP02 DC1116 IG-XL Version: 3.50.40IP02 DIB: P/N 51745600 S/N xxx Rev 0901A

%INFO - ----------
%INFO - System IP750_xxxE (IP750EX)
%INFO - IG-XL 3.50.40IP02, Build: 04.13.11.20.00
%INFO - Maintenance 7.60.40IP02, Build: 04.18.11.02.09
%INFO - ----------
- Starting APMU PG test
- Starting PG_History_Ram
- Completed PG_History_Ram
- Starting PG_Svm_Ram
- Completed PG_Svm_Ram
- Starting PG_Scramble_Ram, ADSS
- Completed PG_Scramble_Ram
- Starting PG_Scramble_Ram, Tset
- Completed PG_Scramble_Ram
- Starting PG_LVM_BIST_Ram (up to 32 sec)
- Completed PG_LVM_BIST_Ram in 21.6 sec
- Completed APMU PG test
-
- Starting APMU IDPROM test
- APMU Mother Board - P/N:51740001 Rev:1012A S/N: 4
- APMU Relay Board - P/N:51740200 Rev:2060 S/N: 25
- APMU Rider Board - P/N:51740100 Rev:5200 S/N: 25
- APMU Rider Board - P/N:51740100 Rev:5200 S/N: 25
- APMU Rider Board - P/N:51740100 Rev:5200 S/N: 25
- APMU Rider Board - P/N:51740100 Rev:5200 S/N: 250
- APMU Rider Board - P/N:51740100 Rev:5200 S/N: 2508
- APMU Rider Board - P/N:51740100 Rev:5200 S/N: 250
- APMU Rider Board - P/N:51740100 Rev:5200 S/N: 24
- APMU Rider Board - P/N:51740100 Rev:5200 S/N: 25
- Completed APMU IDPROM test
-
- Starting APMU Register test
- Starting APMU Misc FPGA Register test

- Completed APMU Misc FPGA Register test
- Starting APMU Control FPGA Register test
- Completed APMU Control FPGA Register test
- Completed APMU Register test
-
- Starting APMU Thermal meter test
- Completed APMU Thermal meter test
-
- Starting APMU Voltages test
- Completed APMU Voltages test
-
- Start APMU Reference DAC test
- Complete APMU Reference DAC test
-
- Starting APMU Relay test
- Starting -VMBUS_H- test
- Completed -VMBUS_H- test
- Starting -VMBUS_L- test
- Completed -VMBUS_L- test
- Starting -CALBUS_HS- test
- Completed -CALBUS_HS- test
- Starting -CalBUS resistor- test
- Completed -CalBUS resistor- test
- Completed APMU Relay test

- Starting APMU Analog function test
- Starting -Gate Control- test
- Completed -Gate Control- test
- Starting -Parallel Site- test
- Completed -Parallel Site- test
- Starting -Differential Voltage Meter- test
- Completed -Differential Voltage Meter- test
- Starting -MV mode- test
- Completed -MV mode- test
- Starting -FV mode- test
- Completed -FV mode- test
- Starting -MI mode- test
- Completed -MI mode- test
- Starting -FI mode- test
- Completed -FI mode- test
- Starting -Clamp I mode- test
- Completed -Clamp I mode- test
- Starting -Clamp V mode- test
- Completed -Clamp V mode- test
- Starting -Gang_FV(8ch) mode- test
- Completed -Gang_FV(8ch) mode- test
- Starting -Gang_FI(8ch) mode- test
- Completed -Gang_FI(8ch) mode- test
- Completed APMU Analog function test

%JOB_END - ****PASSED**** APMU Quick Check of slot 5 (S/N:40) at 12:05:43 PM